FIG. 1

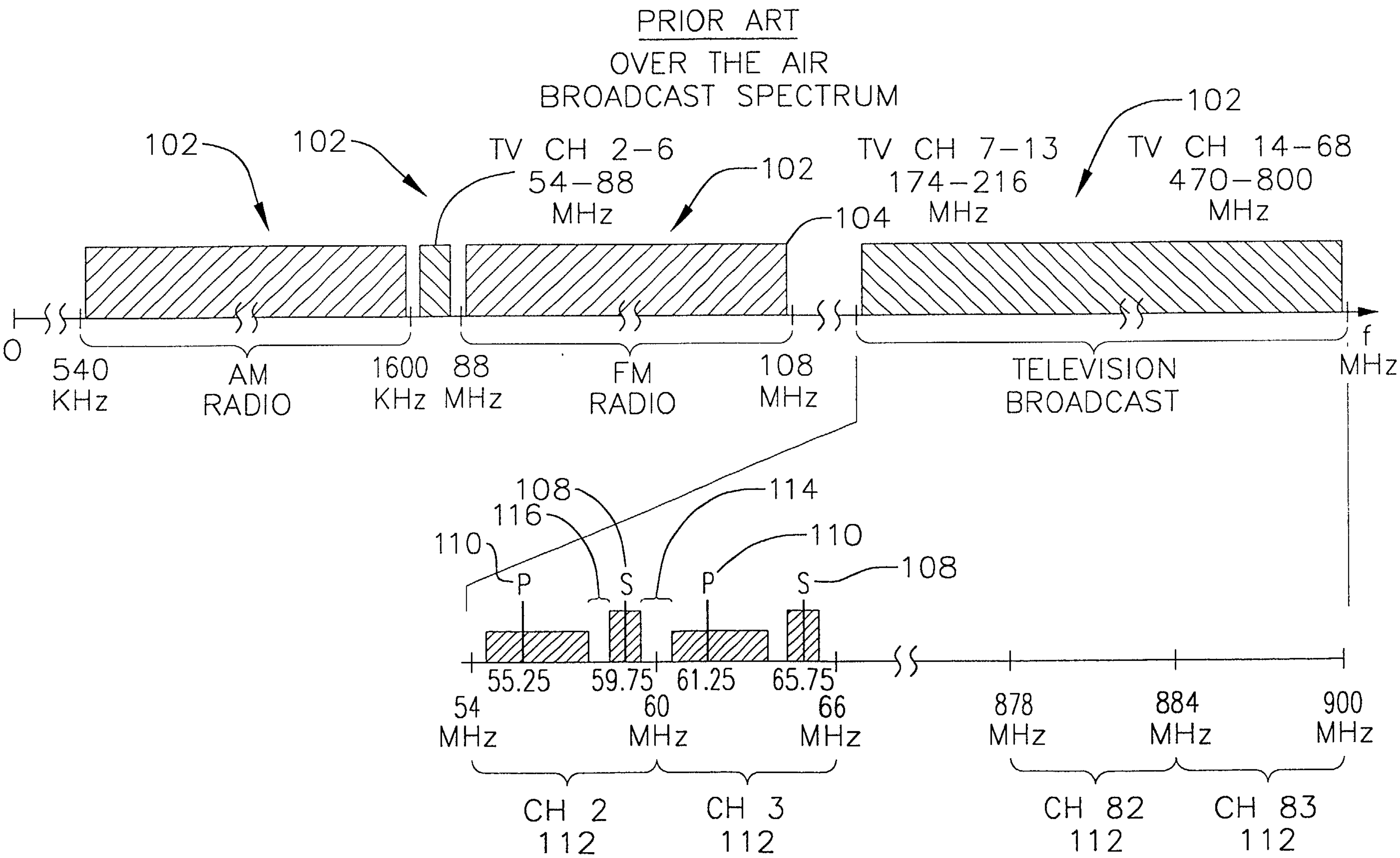

PRIOR ART
OVER THE AIR
BROADCAST SPECTRUM
102
102
TV CH 2-6
54-88
MHz
102
104
TV CH 7-13
174-216
MHz
102
TV CH 14-68
470-800
MHz
O
540
KHz
AM
RADIO
1600
KHz
88
MHz
FM
RADIO
108
MHz
TELEVISION
BROADCAST
f
MHz
108
116
110
114
110
108
P
S
P
S
55.25
59.75
61.25
65.75
54
MHz
60
MHz
66
MHz
878
MHz
884
MHz
900
MHz
CH 2
112
CH 3
112
CH 82
112
CH 83
112

FIG.2

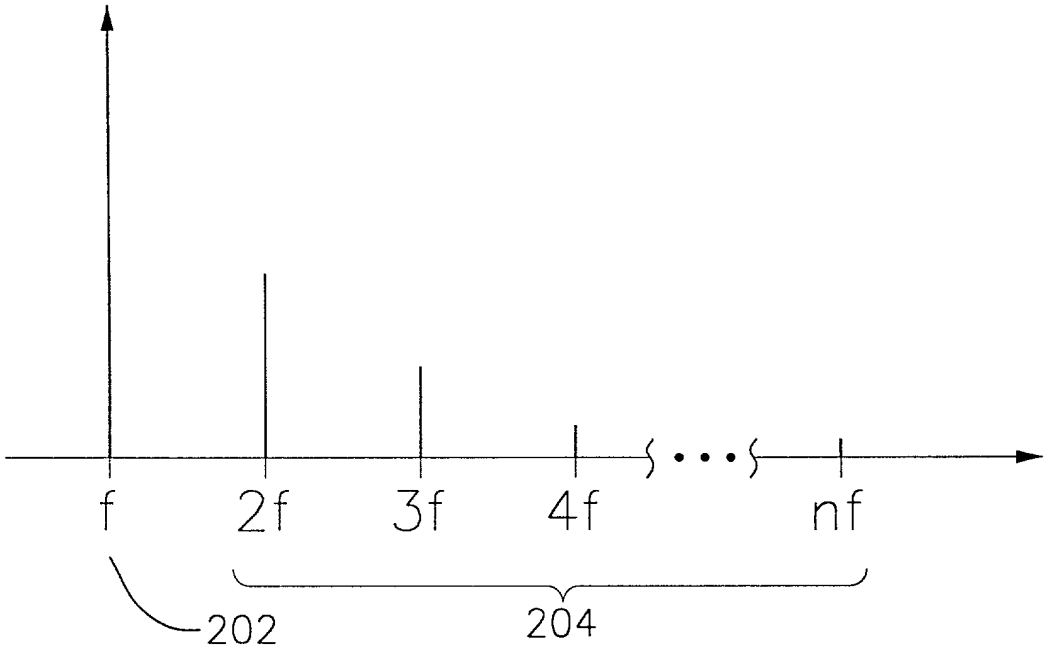


FIG.3

PRIOR ART

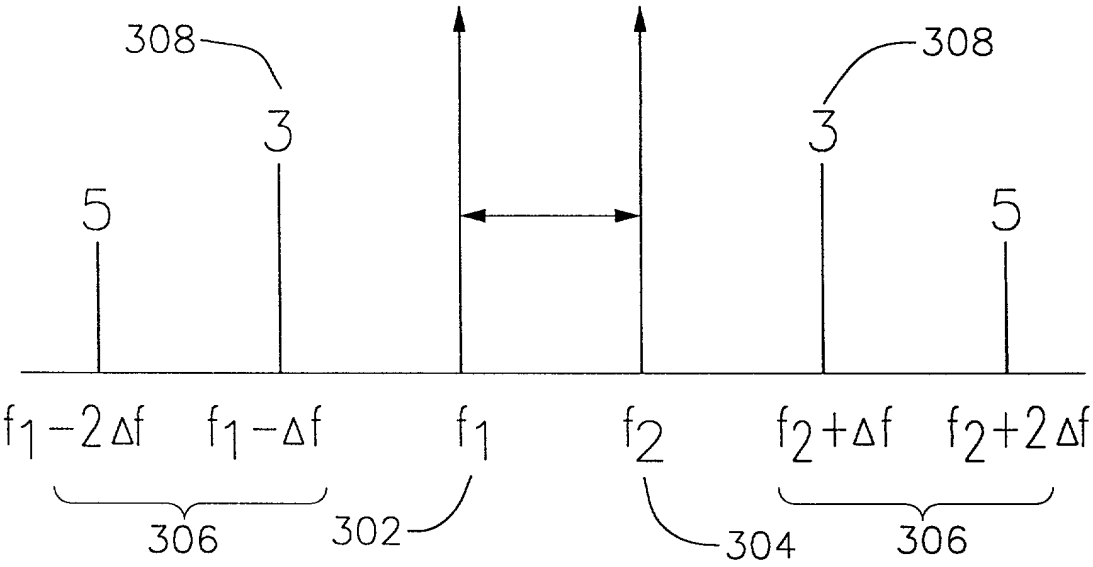


FIG. 4
PRIOR ART

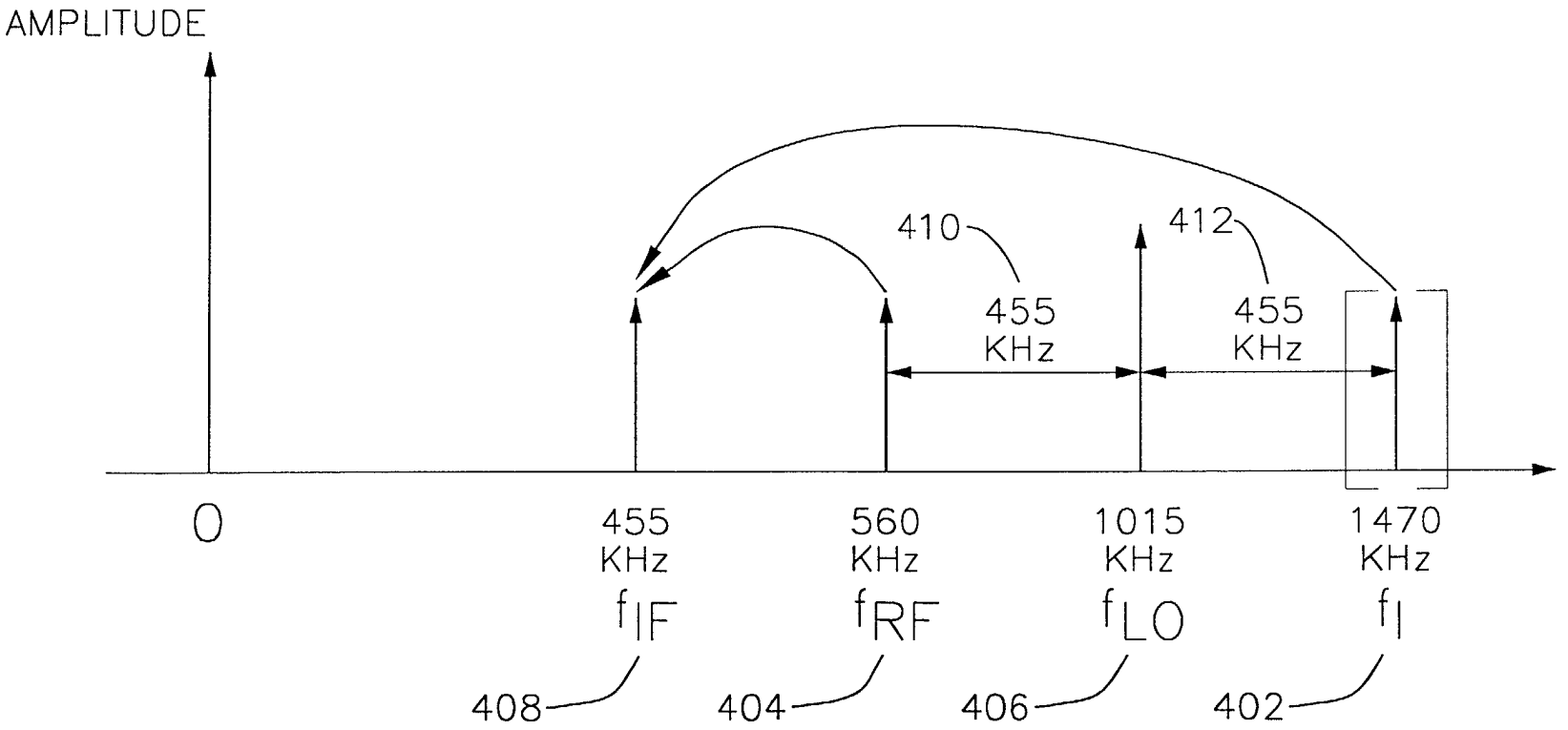
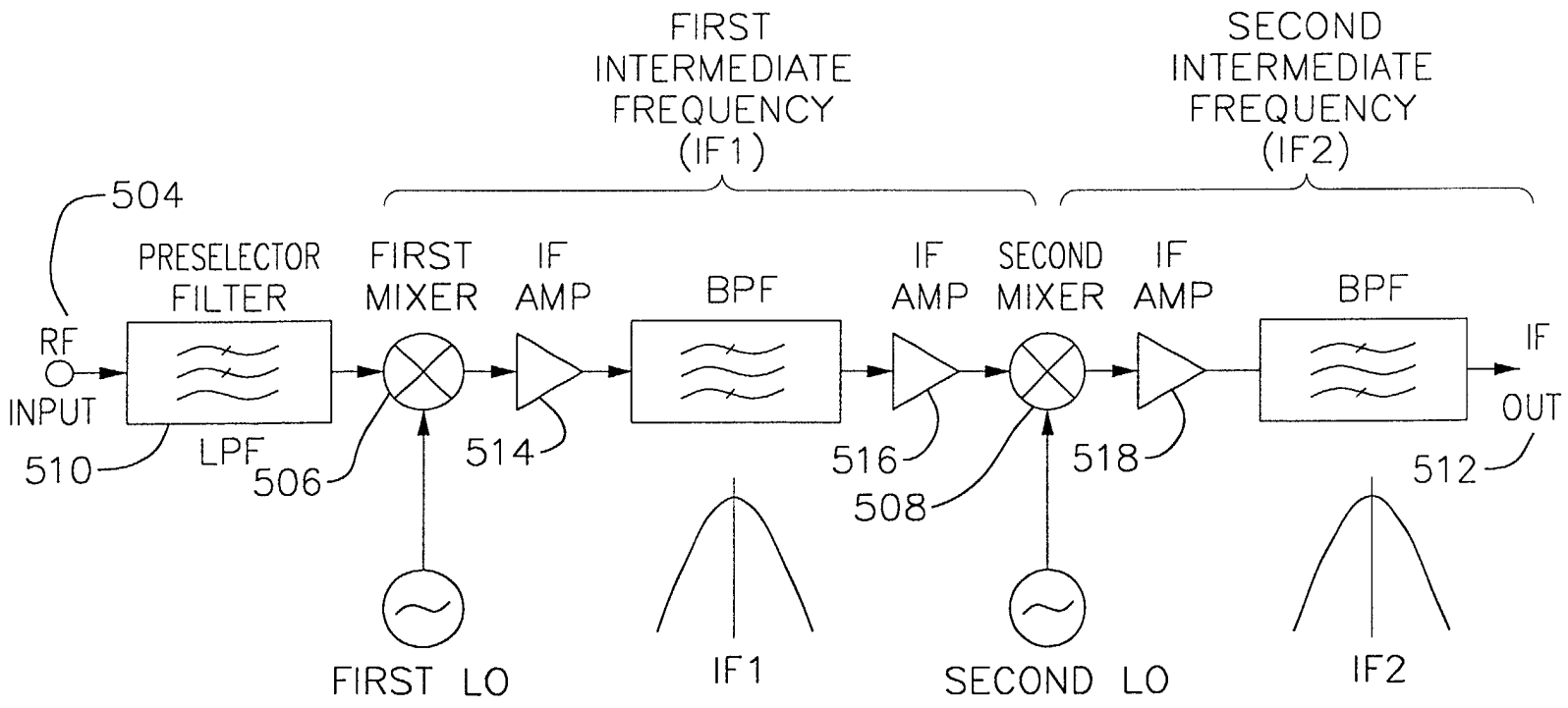


FIG. 5

DUAL CONVERSION RECEIVER



IF2<RFINPUT<IF1

FIG. 6

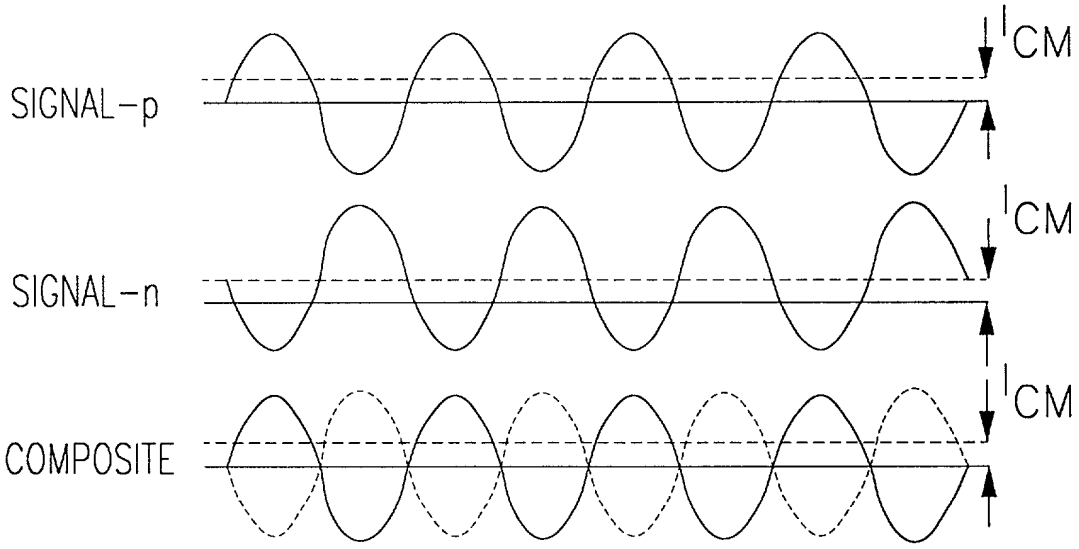

SIGNAL-p
SIGNAL-n
COMPOSITE
I_{CM}
I_{CM}
I_{CM}

FIG. 7

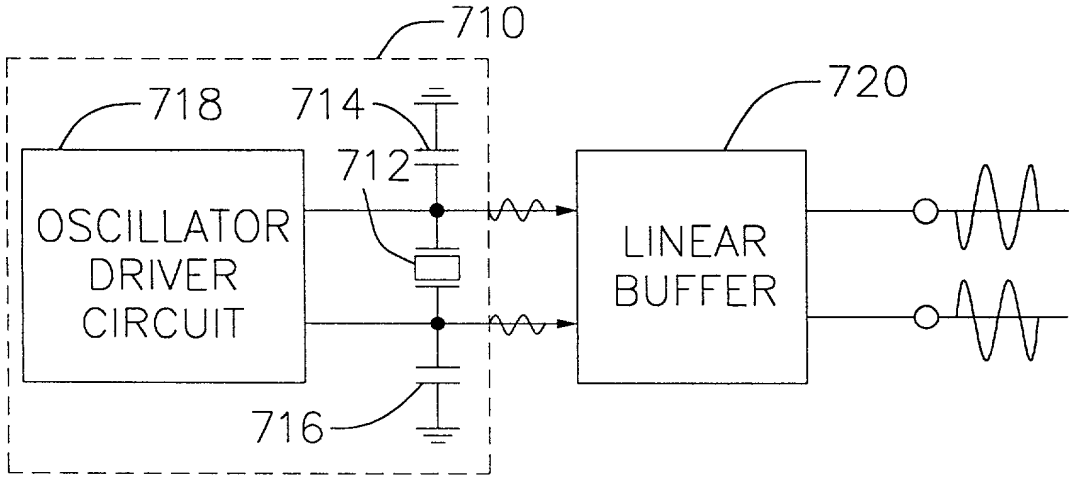

710
718
714
712
716
720
OSCILLATOR DRIVER CIRCUIT
LINEAR BUFFER

FIG. 8

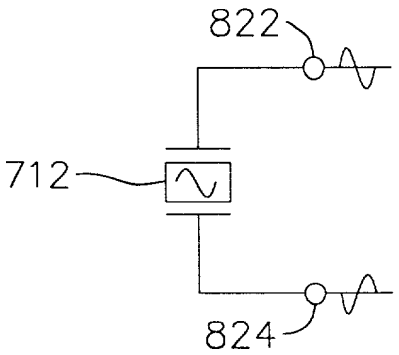


FIG. 9

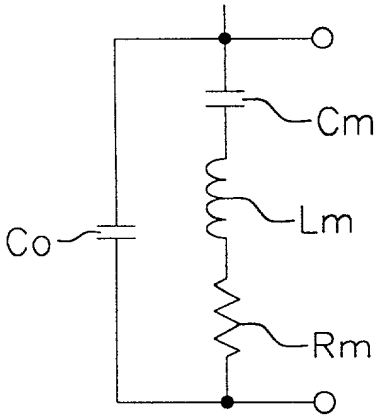


FIG. 10

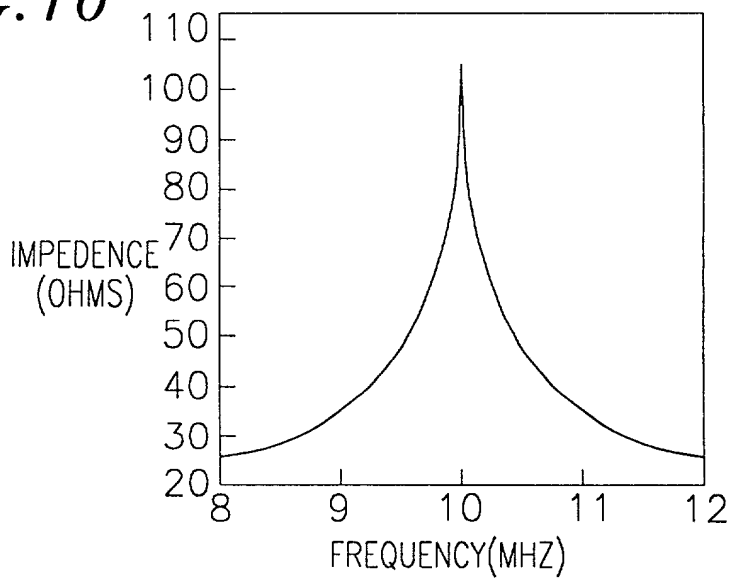


FIG. 11

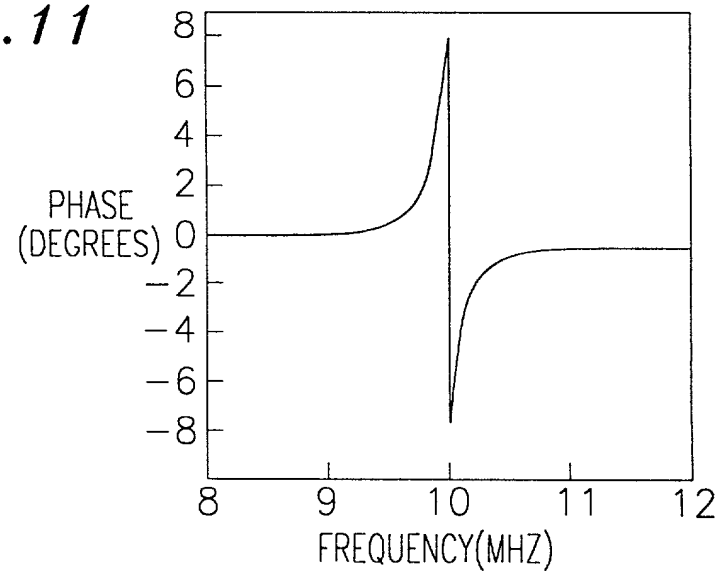


FIG. 12

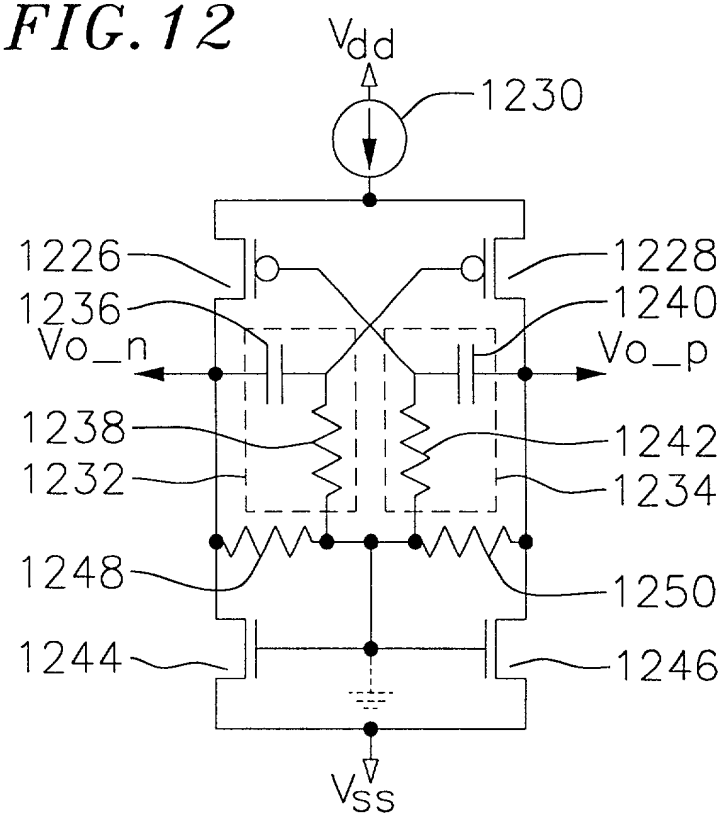

Vdd
1230
1226
1228
1236
1240
Vo_n
Vo_p
1238
1242
1232
1234
1248
1250
1244
1246
Vss

FIG. 13

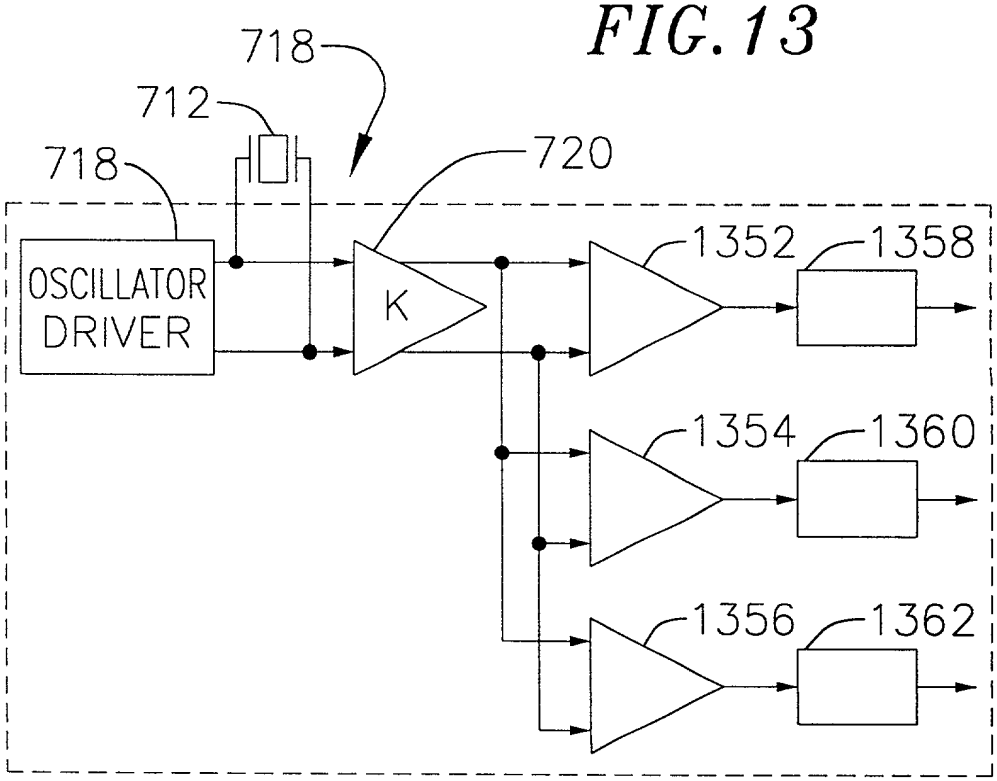

718
712
718
720
OSCILLATOR DRIVER
K
1352
1358
1354
1360
1356
1362

FIG. 14

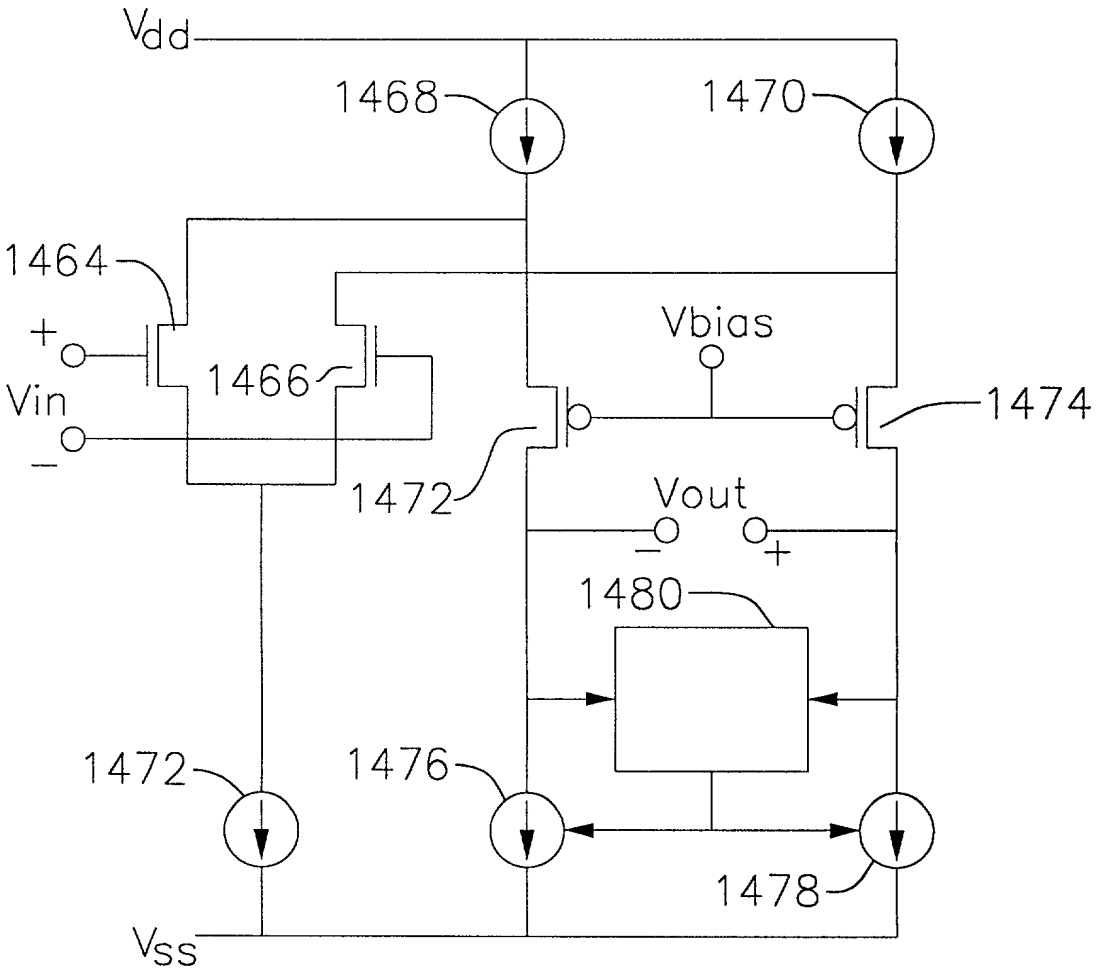

Vdd
1468
1470
1464
+
Vin
−
1466
Vbias
1474
1472
Vout
−
+
1480
1472
1476
1478
Vss

FIG. 15

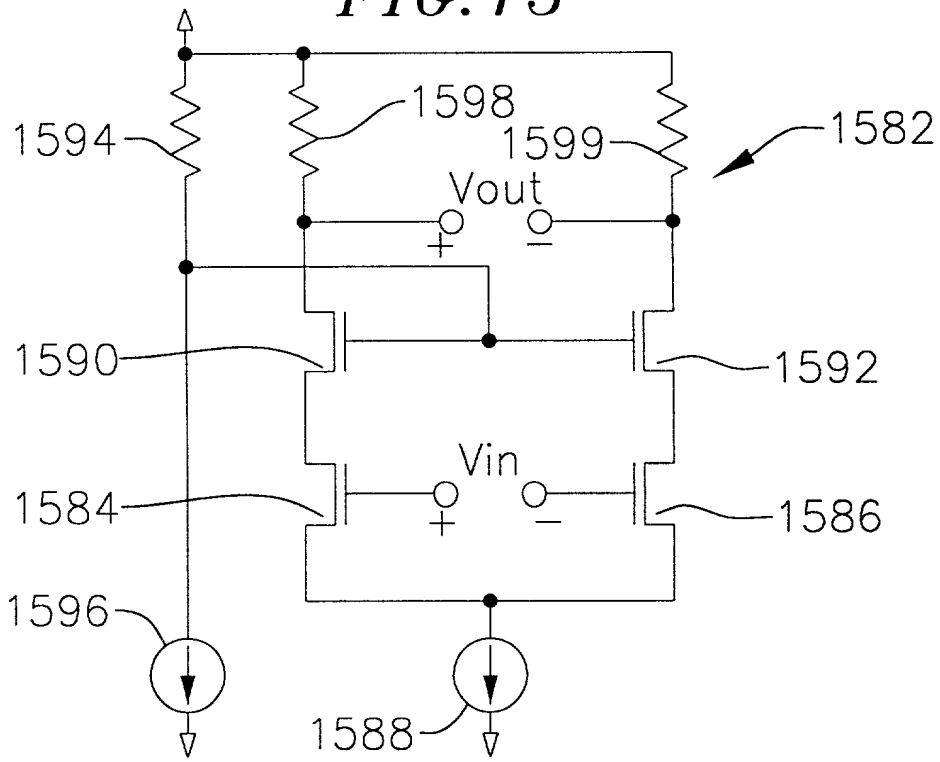

1594
1598
1599
1582
Vout
+
−
1590
1592
Vin
1584
1586
1596
1588

FIG. 16

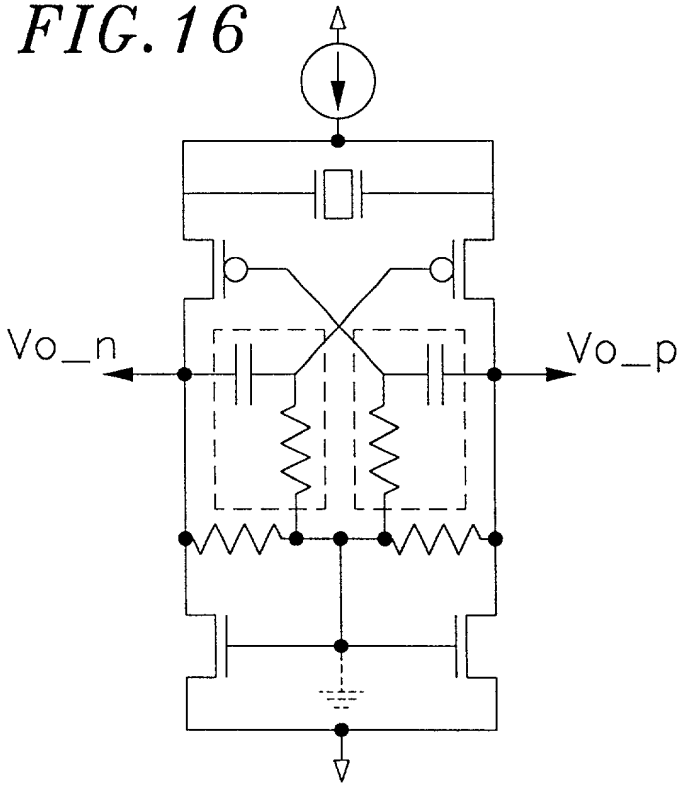

Vo_n
Vo_p

FIG. 17

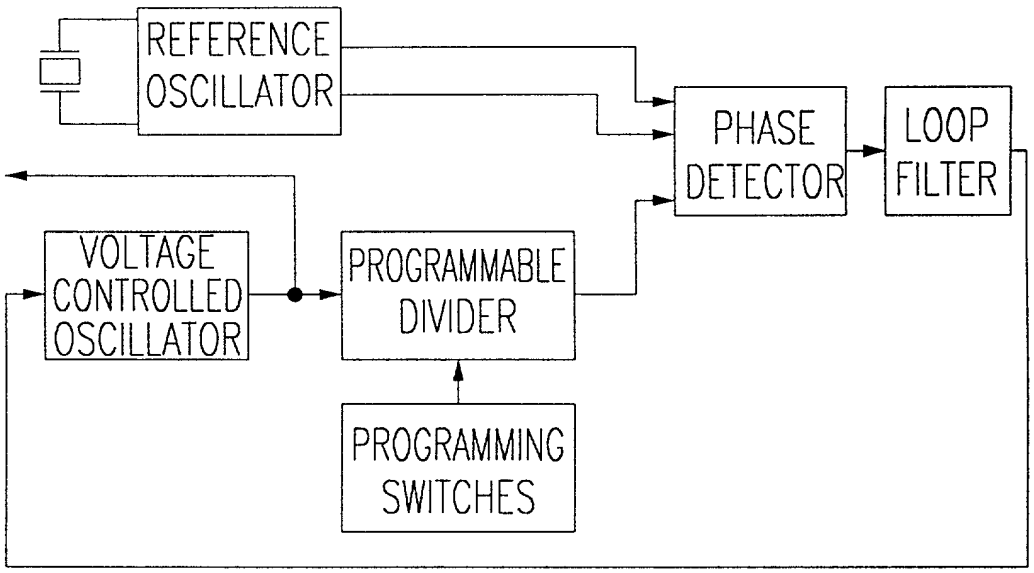

REFERENCE OSCILLATOR
PHASE DETECTOR
LOOP FILTER
VOLTAGE CONTROLLED OSCILLATOR
PROGRAMMABLE DIVIDER
PROGRAMMING SWITCHES

FIG. 18

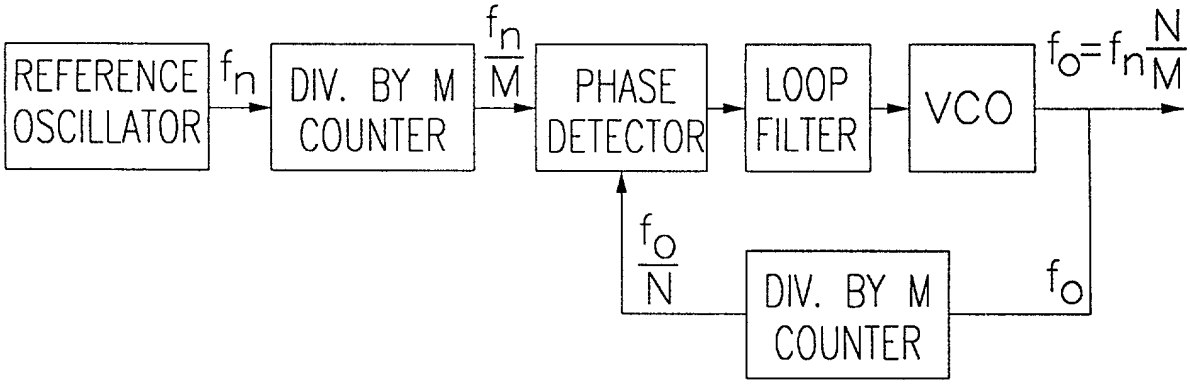

REFERENCE OSCILLATOR
f_n
DIV. BY M COUNTER
$\frac{f_n}{M}$
PHASE DETECTOR
LOOP FILTER
VCO
$f_O = f_n \frac{N}{M}$
$\frac{f_O}{N}$
DIV. BY M COUNTER
f_O

FIG. 19

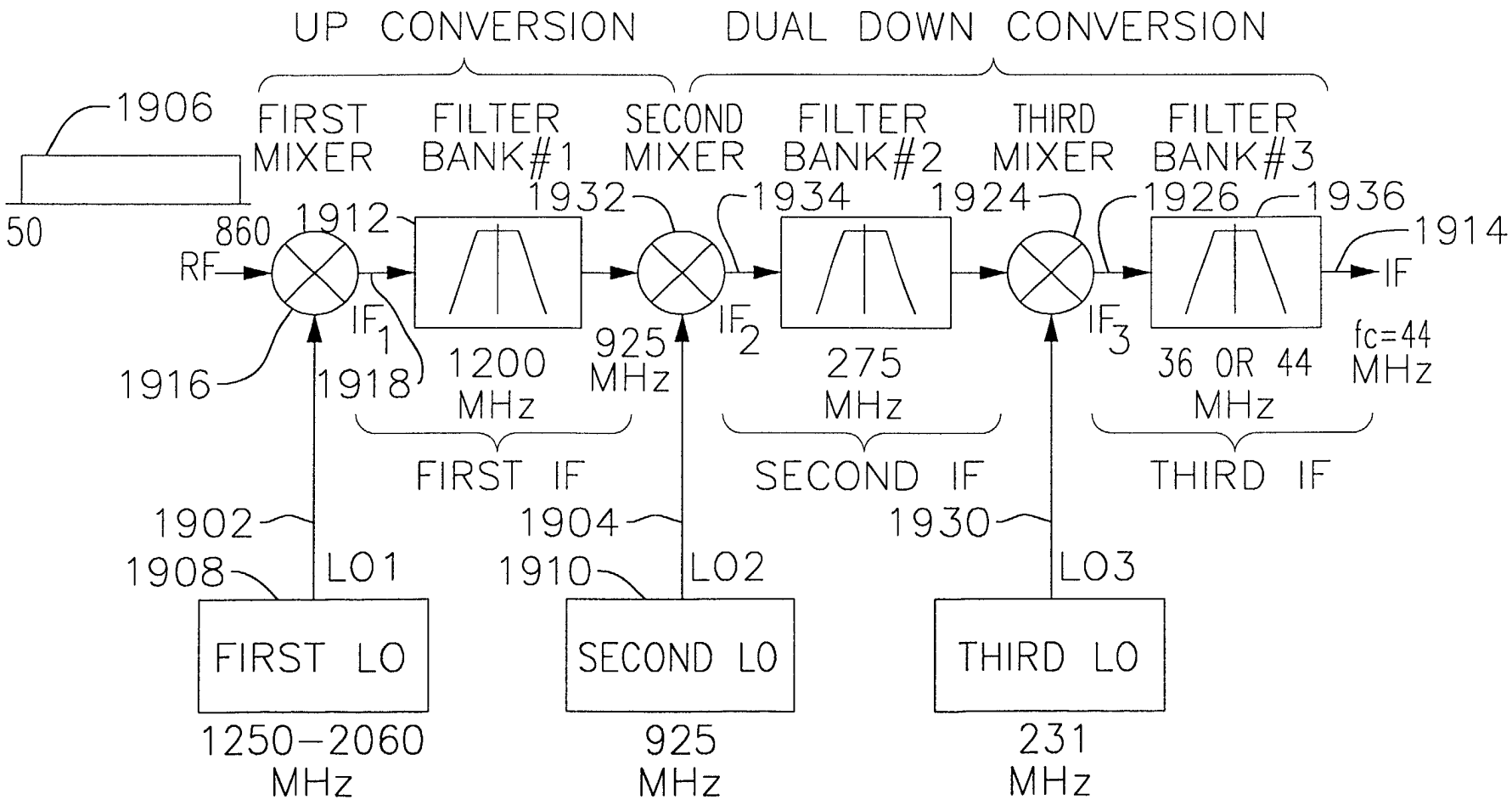
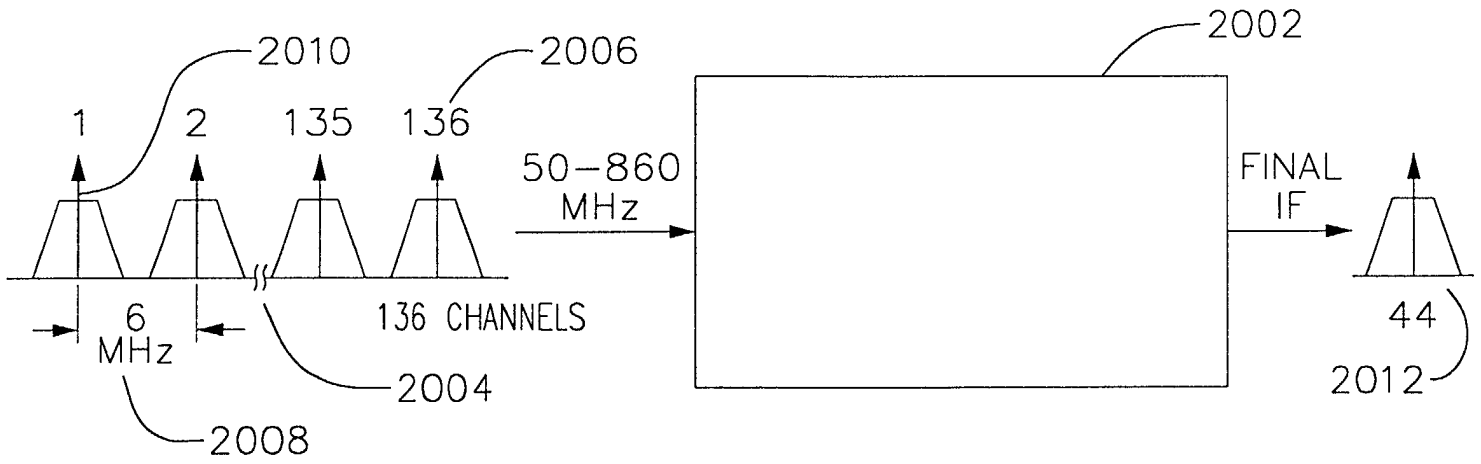

UP CONVERSION
DUAL DOWN CONVERSION
1906
FIRST MIXER
FILTER BANK#1
SECOND MIXER
FILTER BANK#2
THIRD MIXER
FILTER BANK#3
50
860
RF
1912
1932
1934
1924
1926
1936
1914
IF
IF1
IF2
IF3
1916
1918
1200 MHz
925 MHz
275 MHz
36 OR 44 MHz
fc=44 MHz
FIRST IF
SECOND IF
THIRD IF
1902
1904
1930
1908
LO1
1910
LO2
LO3
FIRST LO
SECOND LO
THIRD LO
1250–2060 MHz
925 MHz
231 MHz

FIG.20



PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

FIG.21

44MHz IF

NOTE
- LO-2 REF=100KHz
  SO DIVIDE RANGE=9216 TO 9280

TABLE OF FREQUENCIES BASED ON COARSE/FINE PLL SOLUTION:

Frf (MHz)	50	56	62	68	74	80	86	92	98	104	110	116	122	128	"	854	860
LO-1 (MHz)	1250	1260	1260	1270	1270	1280	1290	1290	1300	1300	1310	1320	1320	1330	"	2050	2060
IF-1 (MHz)	1200	1204	1198	1202	1196	1200	1204	1198	1202	1196	1200	1204	1198	1202	"	1196	1200
LO-2 (MHz)	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	921.6	924.8	928.0	923.2	926.4	"	921.6	924.8
IF-2 (MHz)	275.2	276	274.8	275.6	274.4	275.2	276.0	274.8	275.6	274.4	275.2	276.0	274.8	275.6	"	274.4	275.2
LO-3 (MHz)	231.2	232	230.8	232	230	231	232	231	232	230	231	232	231	232	"	230	231
IF-3 (MHz)	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	44.0	"	44.0	44.0

PPL Xtal REFERENCE=10MHz
LO-1, 10MHz FREQUENCY STEPS
LO-2, 100kHz FREQUENCY STEPS

FIG.22

36MHz IF

TABLE OF FREQUENCIES BASED ON
COARSE/FINE PLL SOLUTION:

NOTE
- LO-2 REF=100KHz
  SO DIVIDE RANGE=9280 TO 9340

Frf (MHz)	50	58	66	74	82	90	98	106	114	122	130	138	146	154	"	852	860
LO-1 (MHz)	1250	1260	1270	1270	1280	1290	1300	1310	1310	1320	1330	1340	1350	1350	"	2050	2060
IF-1 (MHz)	1200	1202	1204	1196	1198	1200	1202	1204	1196	1198	1200	1202	1204	1196	"	1198	1200
LO-2 (MHz)	931.2	932.8	934.4	928.0	930	931	933	934	928.0	930	931	933	934	928.0	"	929.60	931.2
IF-2 (MHz)	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	268.4	268.8	269.2	269.6	268.0	"	268.4	268.8
LO-3 (MHz)	232.8	233.2	233.6	232	232	233	233	234	232	232	233	233	234	232.0	"	232.4	232.8
IF-3 (MHz)	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	36.0	"	36.0	36.0

FIG.23

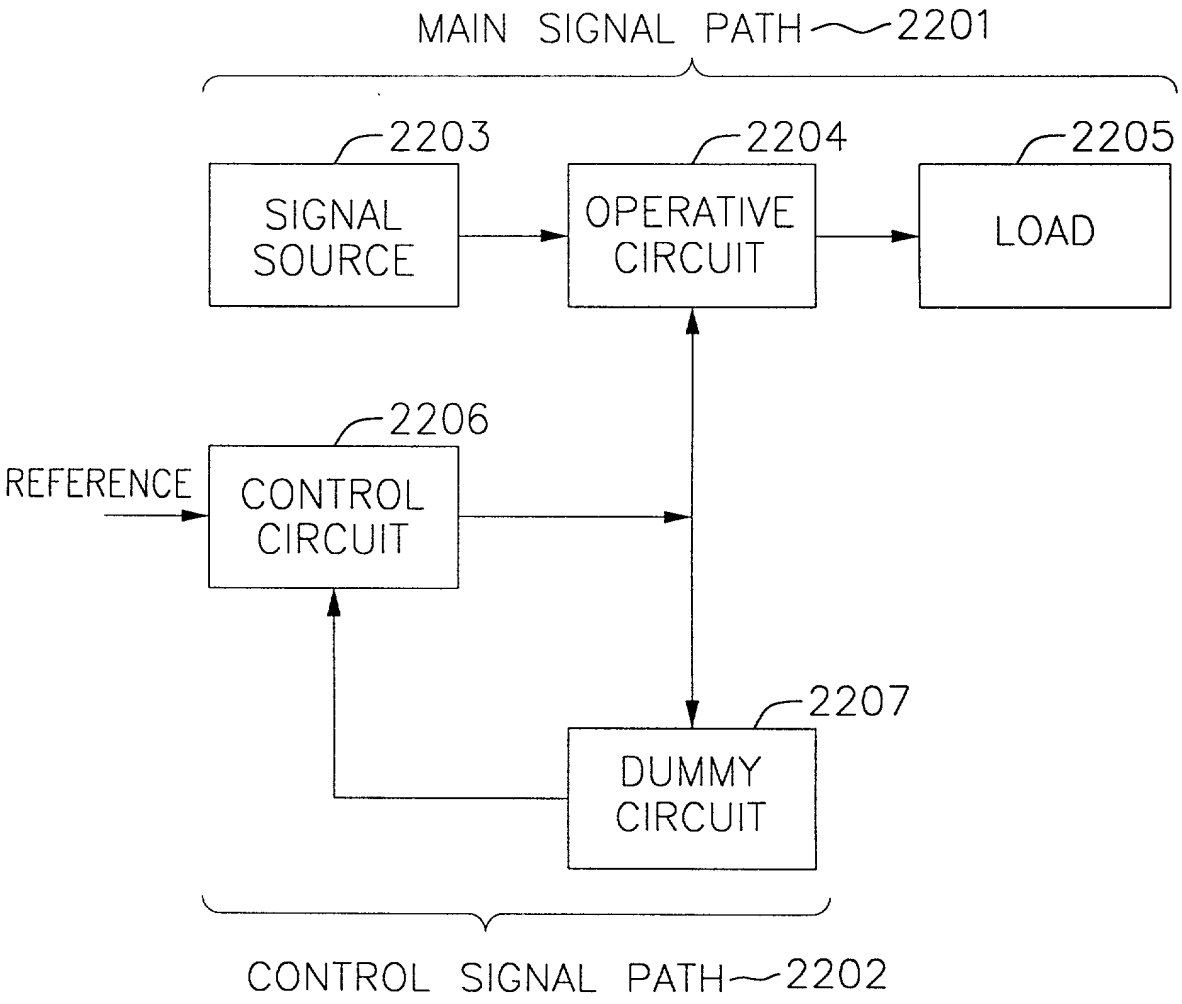

MAIN SIGNAL PATH
2201
2203
2204
2205
SIGNAL SOURCE
OPERATIVE CIRCUIT
LOAD
2206
REFERENCE
CONTROL CIRCUIT
2207
DUMMY CIRCUIT
CONTROL SIGNAL PATH
2202

FIG.24a

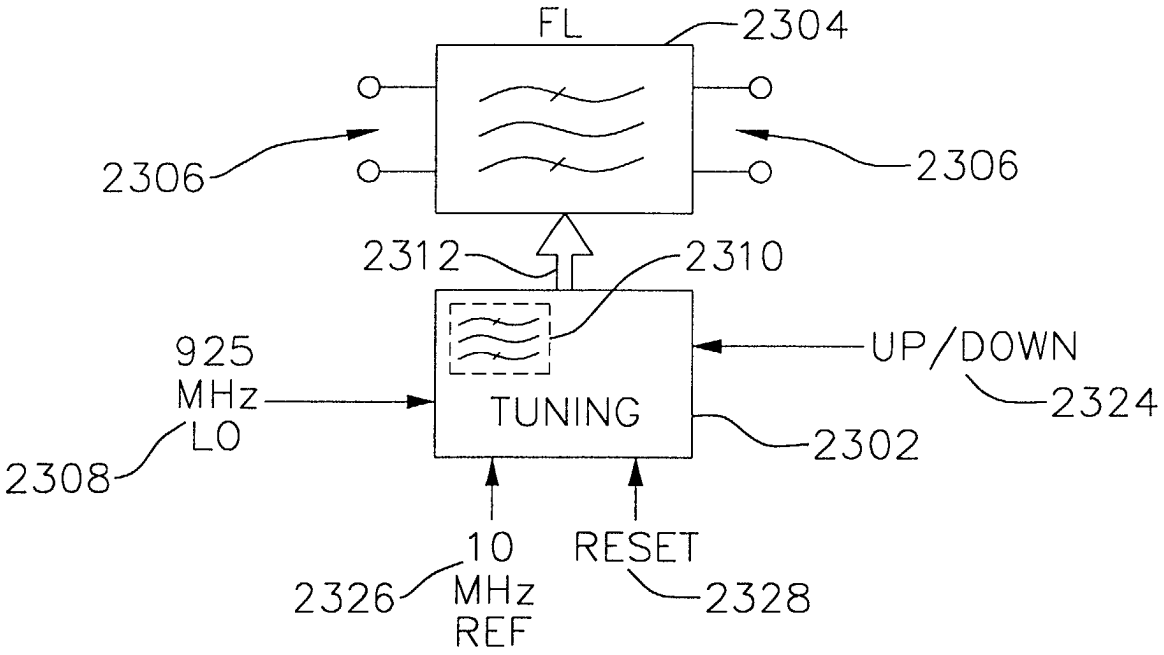


FIG.24b

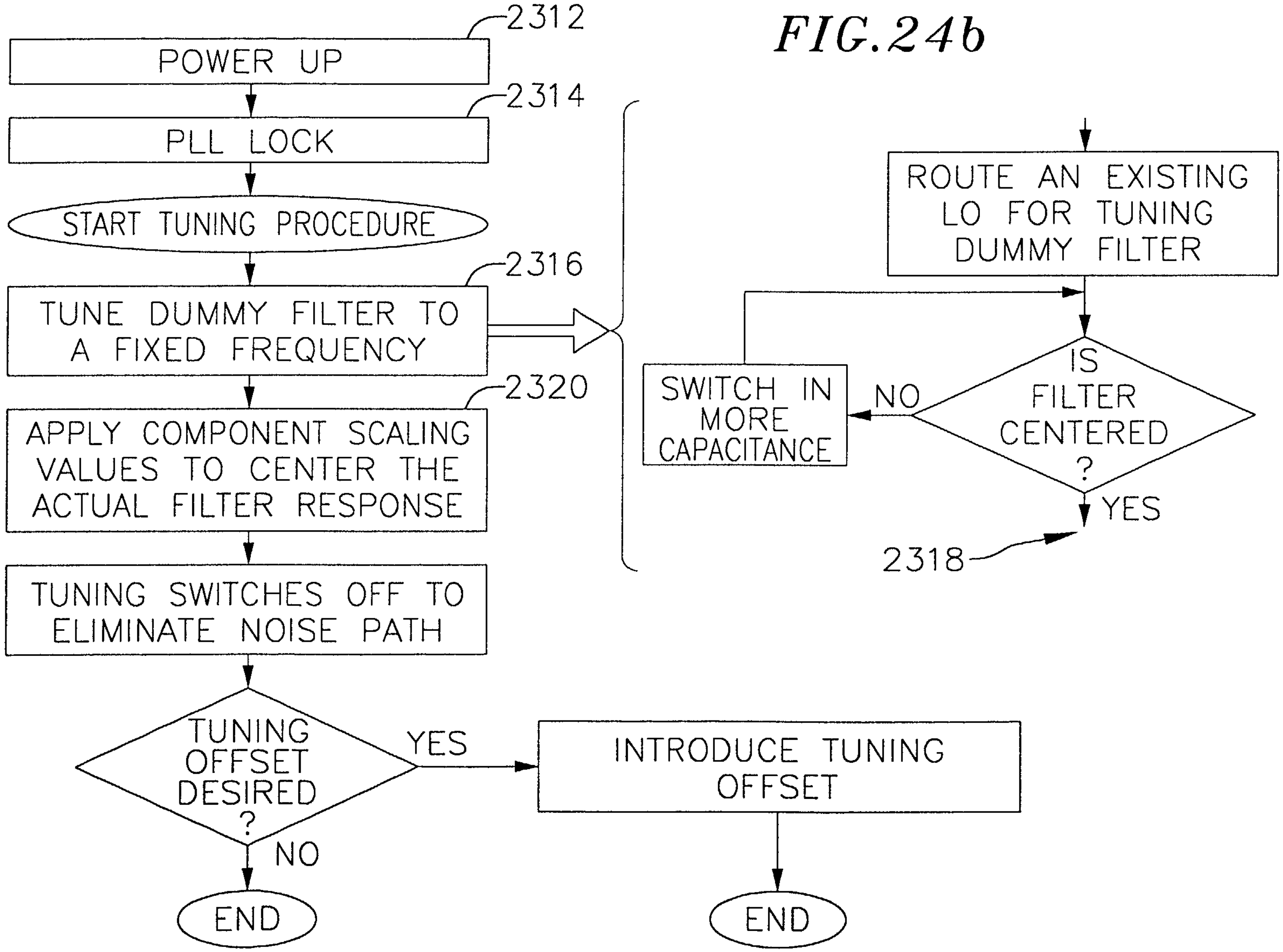

2312
POWER UP
2314
PLL LOCK
START TUNING PROCEDURE
2316
TUNE DUMMY FILTER TO A FIXED FREQUENCY
2320
APPLY COMPONENT SCALING VALUES TO CENTER THE ACTUAL FILTER RESPONSE
TUNING SWITCHES OFF TO ELIMINATE NOISE PATH
TUNING OFFSET DESIRED ?
YES
NO
END
INTRODUCE TUNING OFFSET
END
ROUTE AN EXISTING LO FOR TUNING DUMMY FILTER
IS FILTER CENTERED ?
NO
SWITCH IN MORE CAPACITANCE
YES
2318

FIG.24c

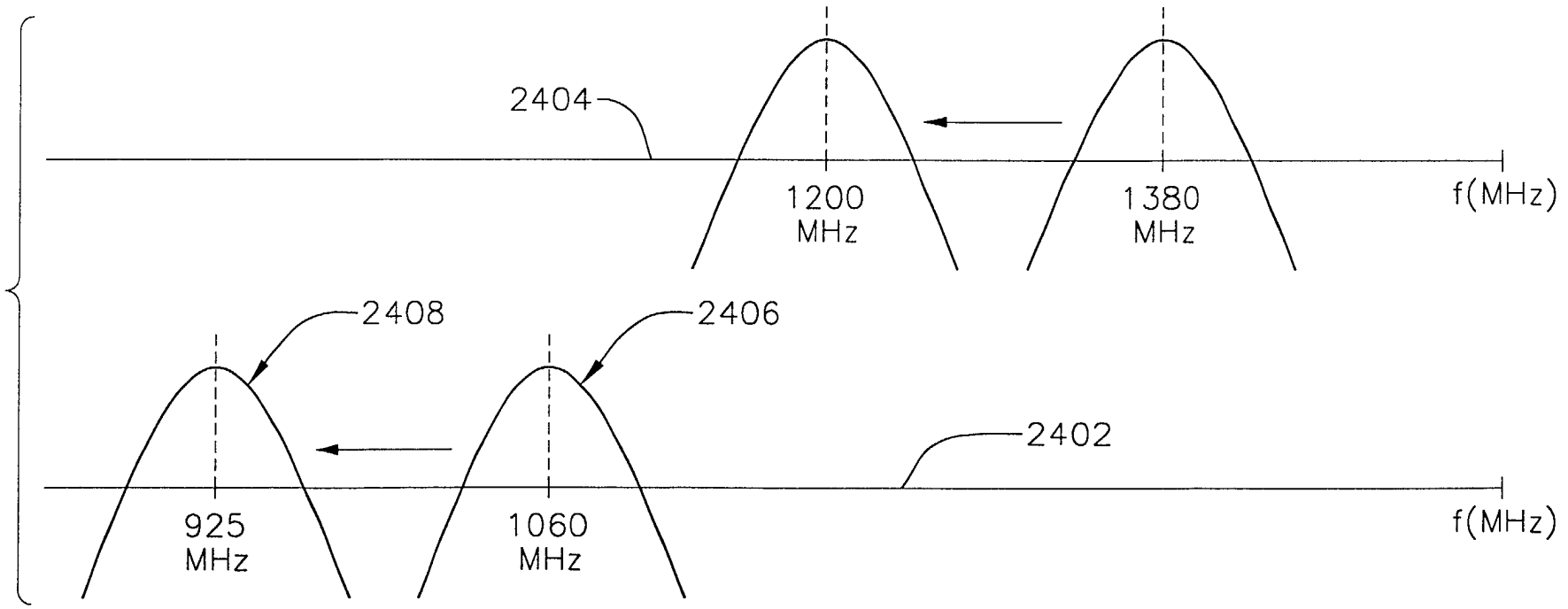


FIG.25

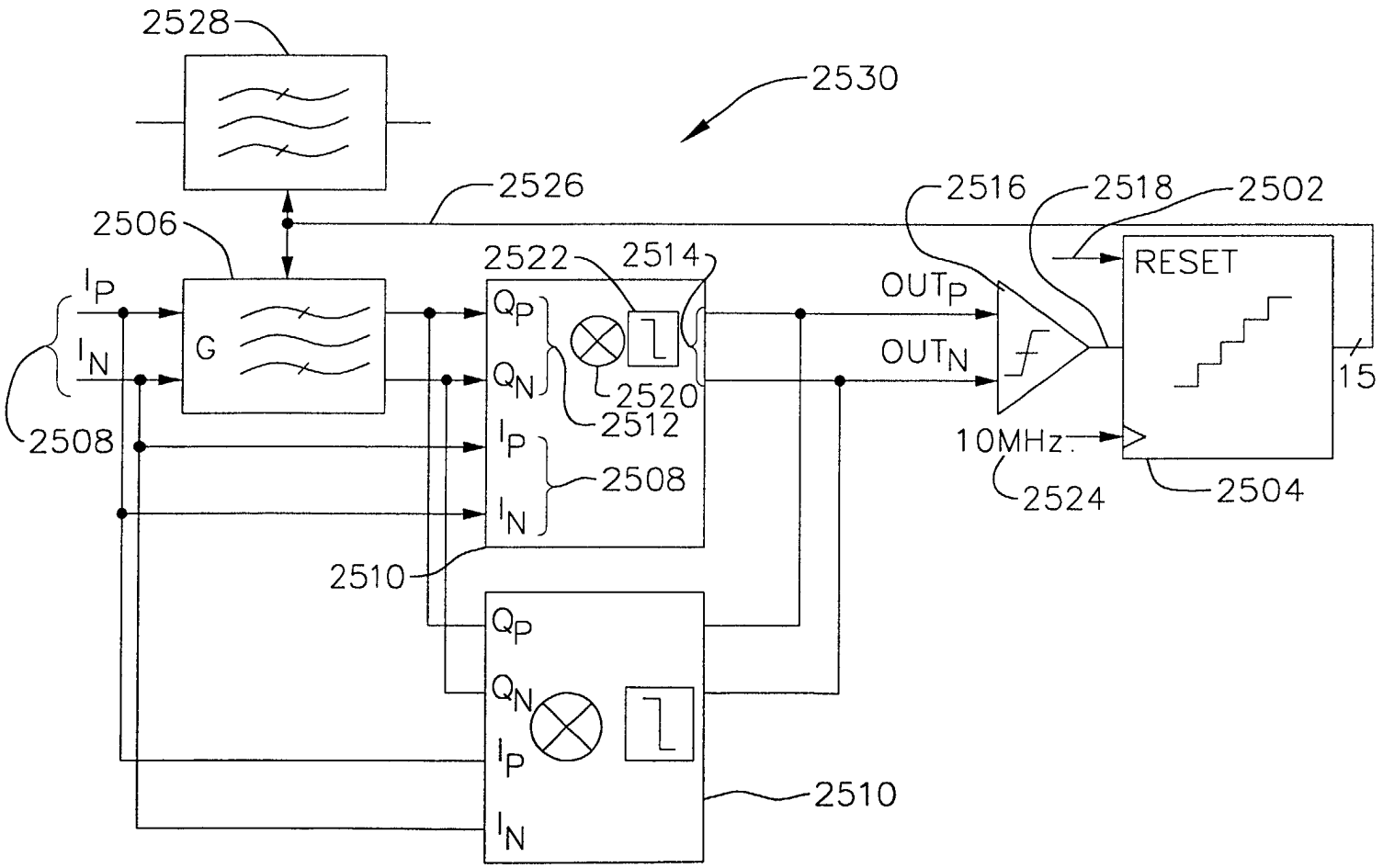


FIG.26

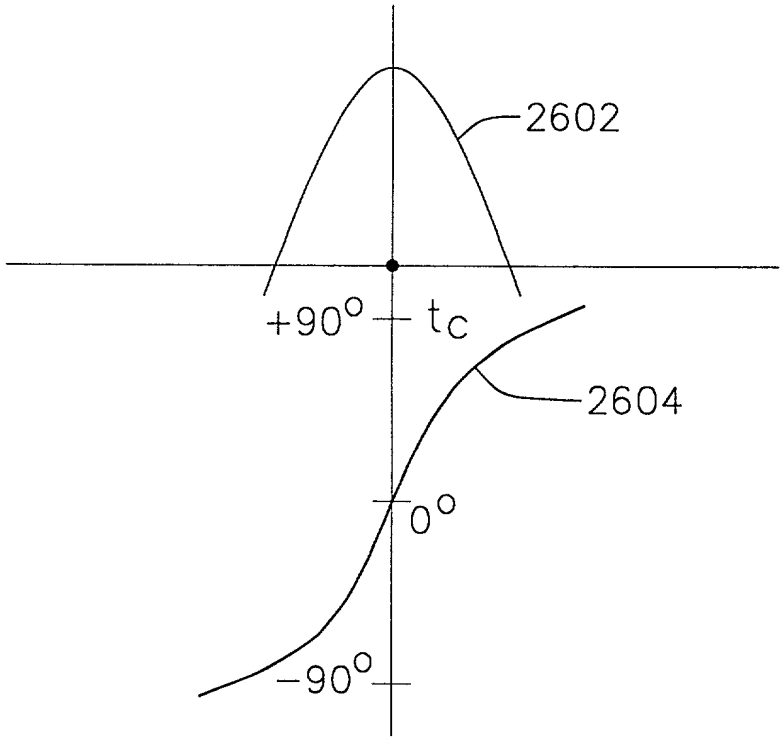


FIG.27

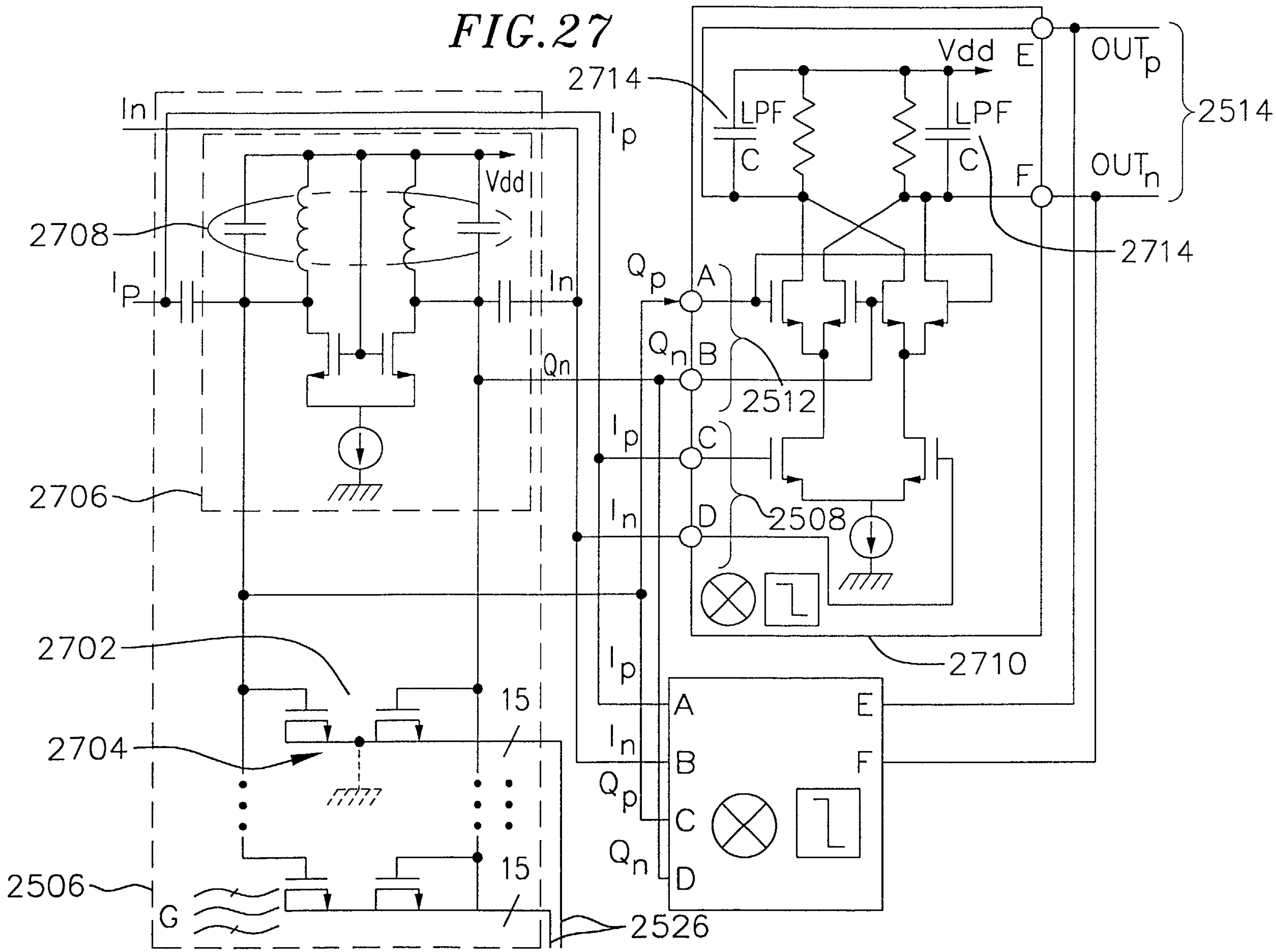
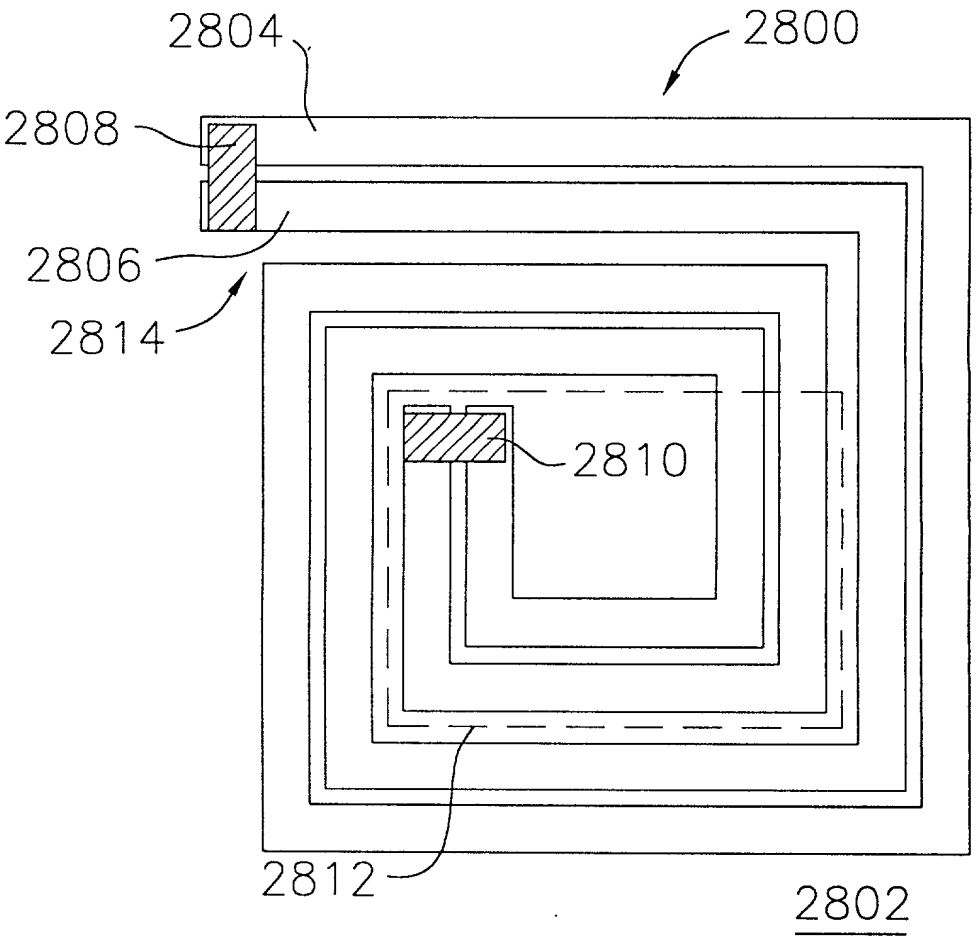

2714
LPF
C
Vdd
E
OUTp
2514
F
OUTn
2714
In
Ip
2708
IP
In
Vdd
Qp
A
Qn
B
Qn
2512
Ip
C
2508
In
D
2706
2710
2702
Ip
A
E
15
2704
In
B
F
Qp
C
Qn
D
2506
15
G
2526

FIG.28a



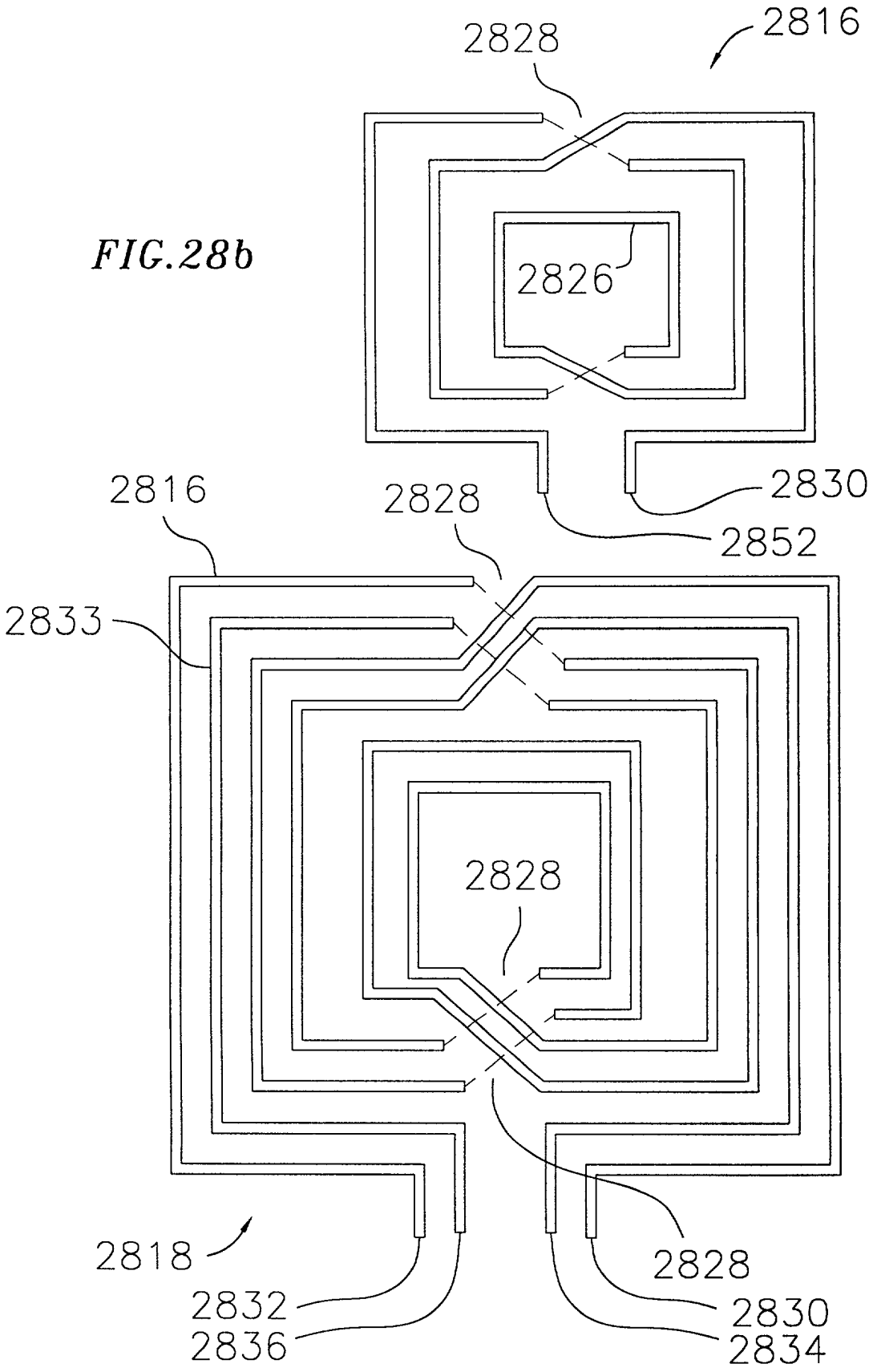
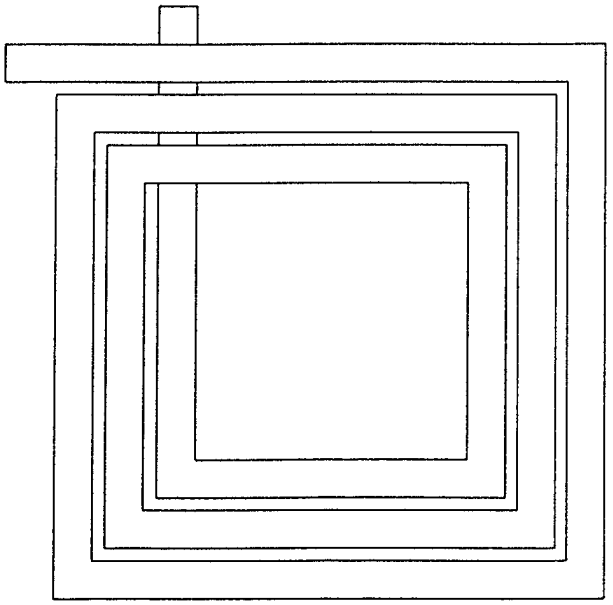

2828
2816
2826
2830
2852
2816
2828
2833
2828
2818
2828
2832
2830
2836
2834

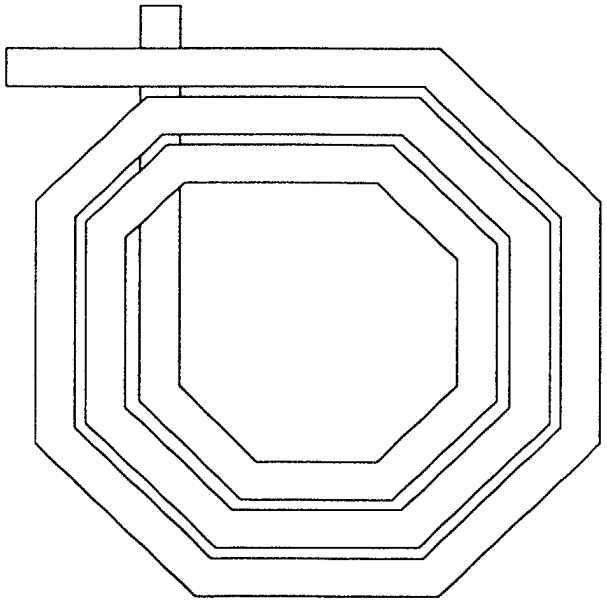
FIG.28b

FIG.28c



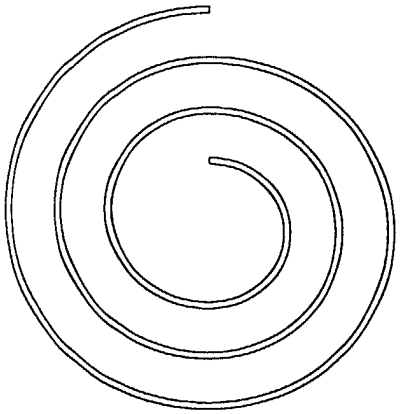
2820

FIG.28d



2822

FIG.28e



2824

FIG.28f

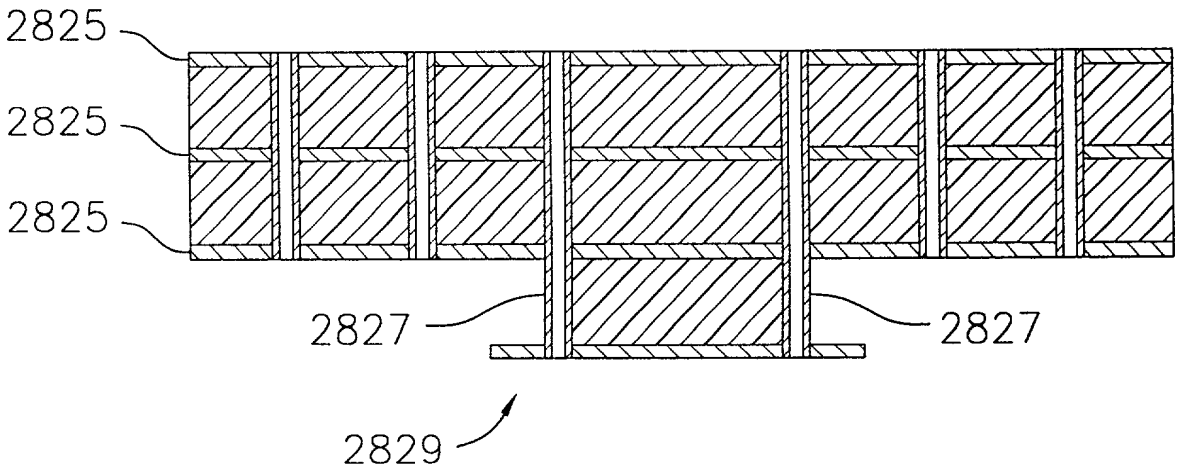


FIG.28g

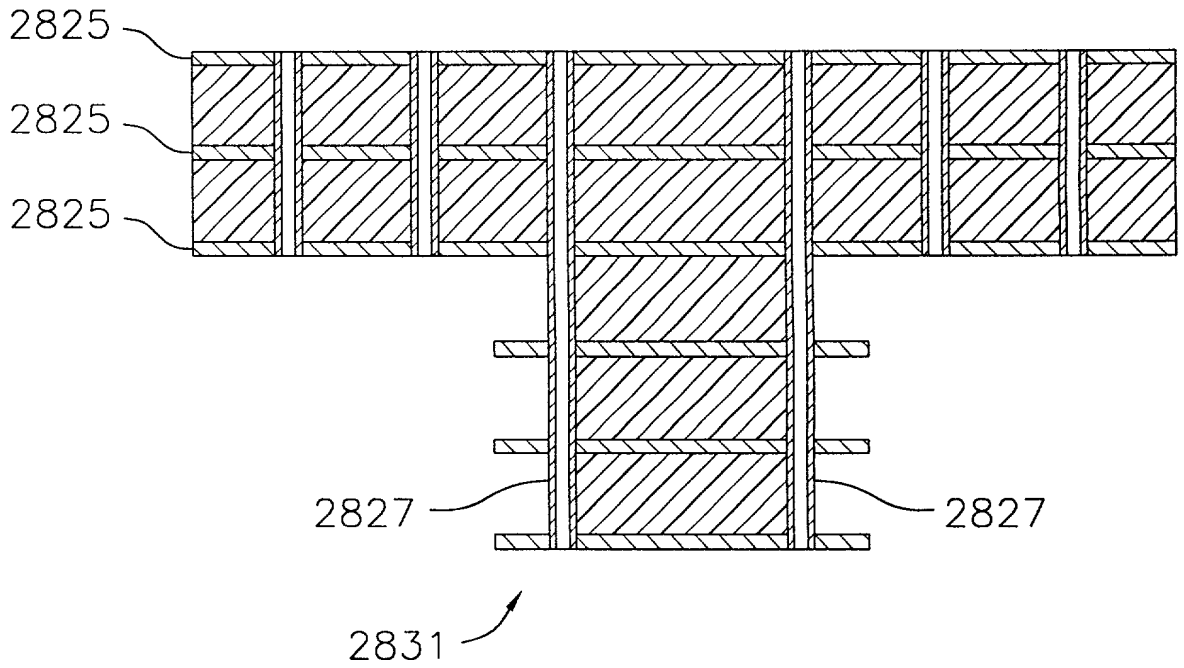


FIG.28h

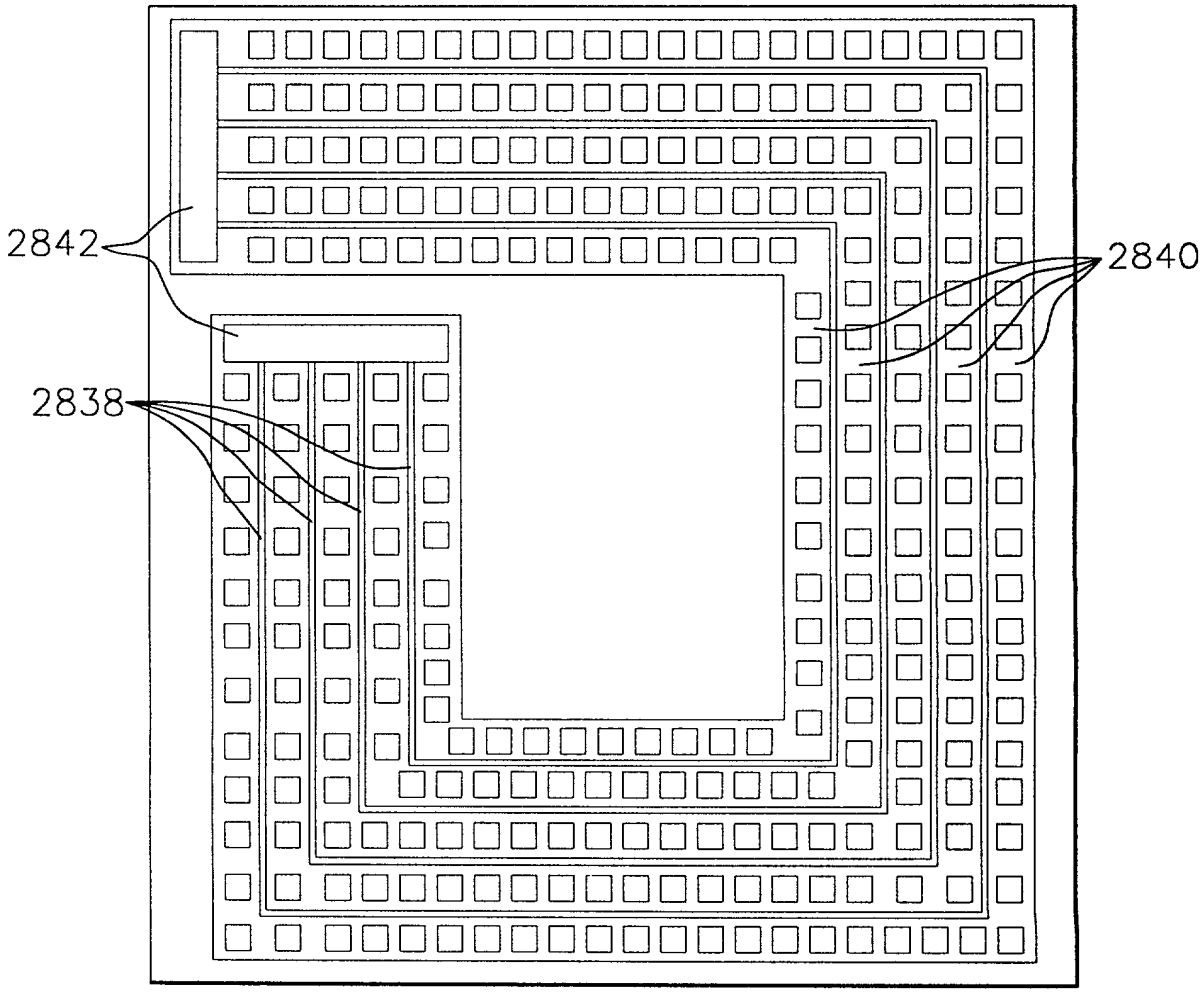


FIG.28i

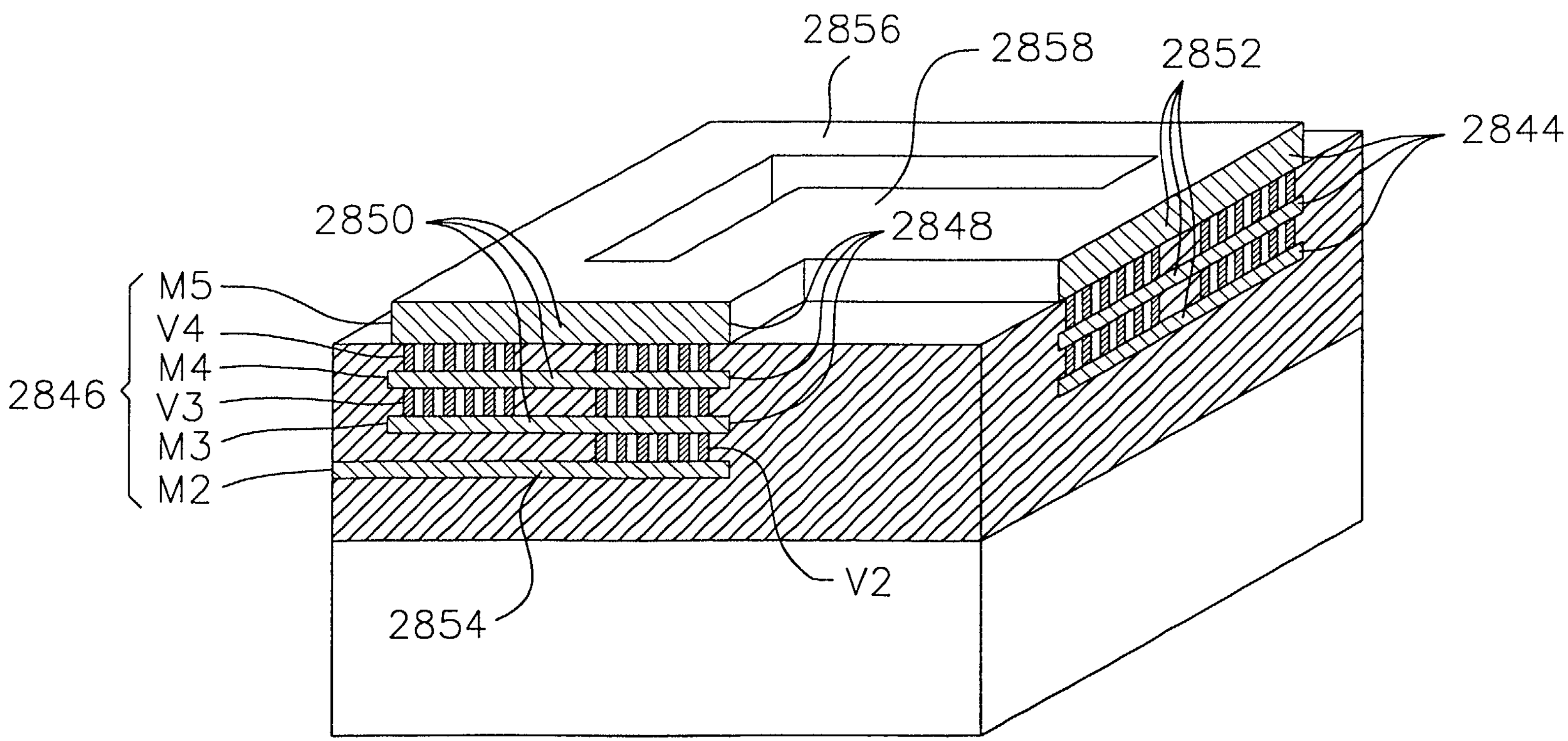


FIG.28j

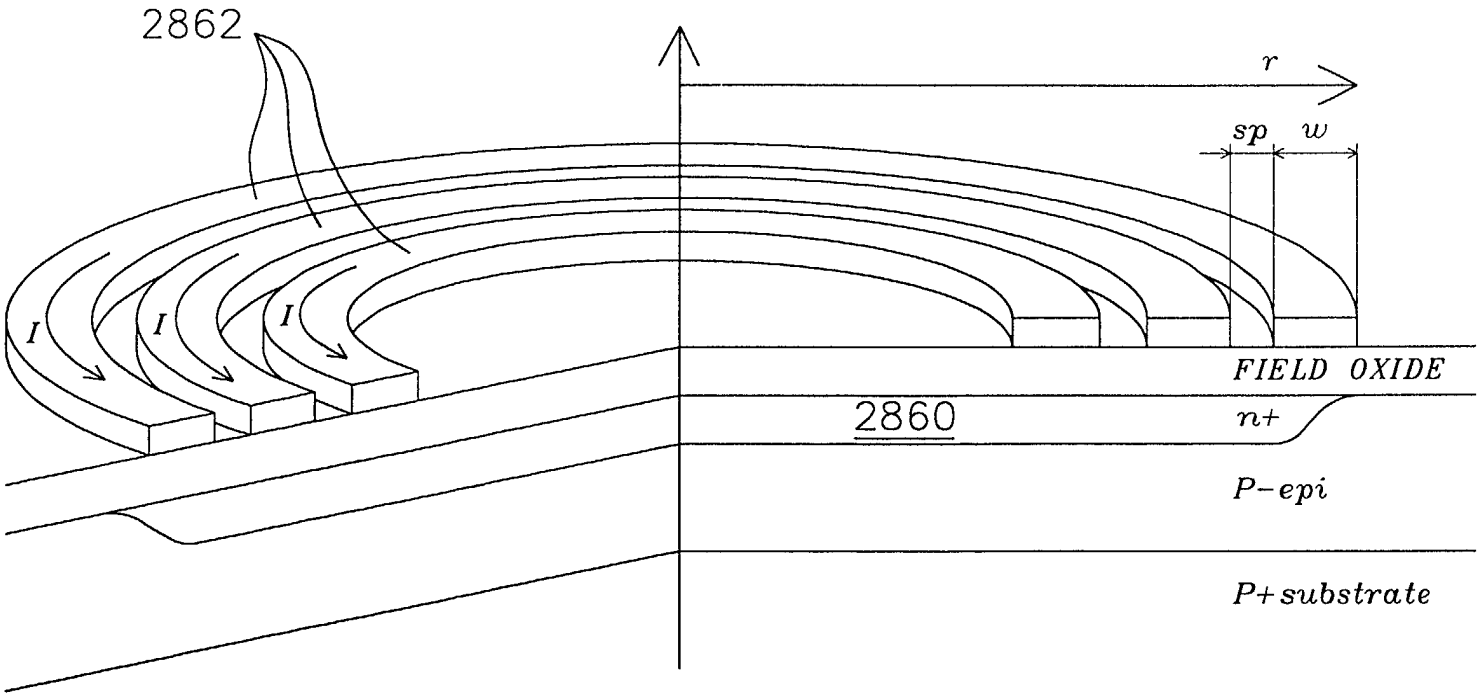


FIG.28k

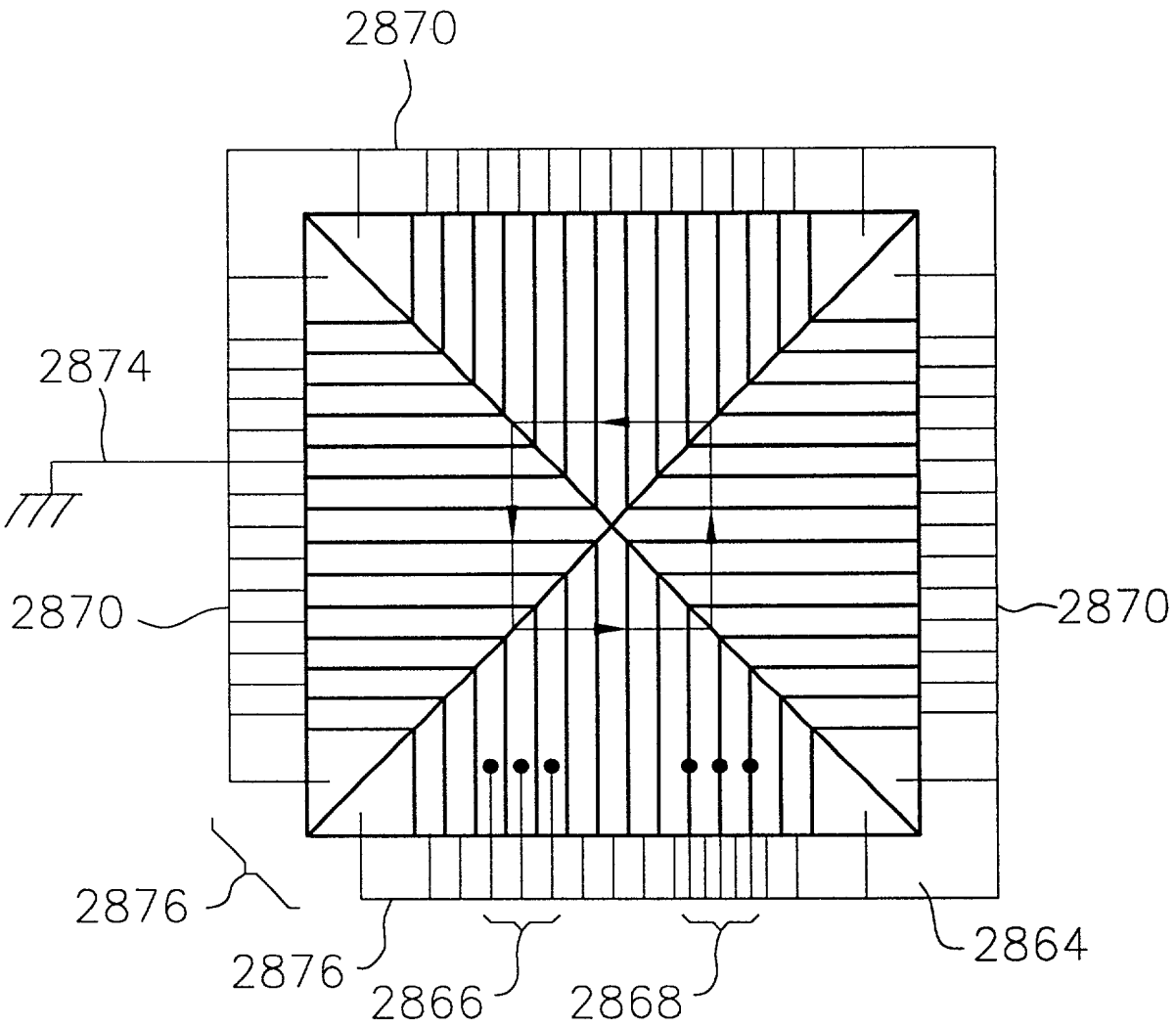


FIG.29

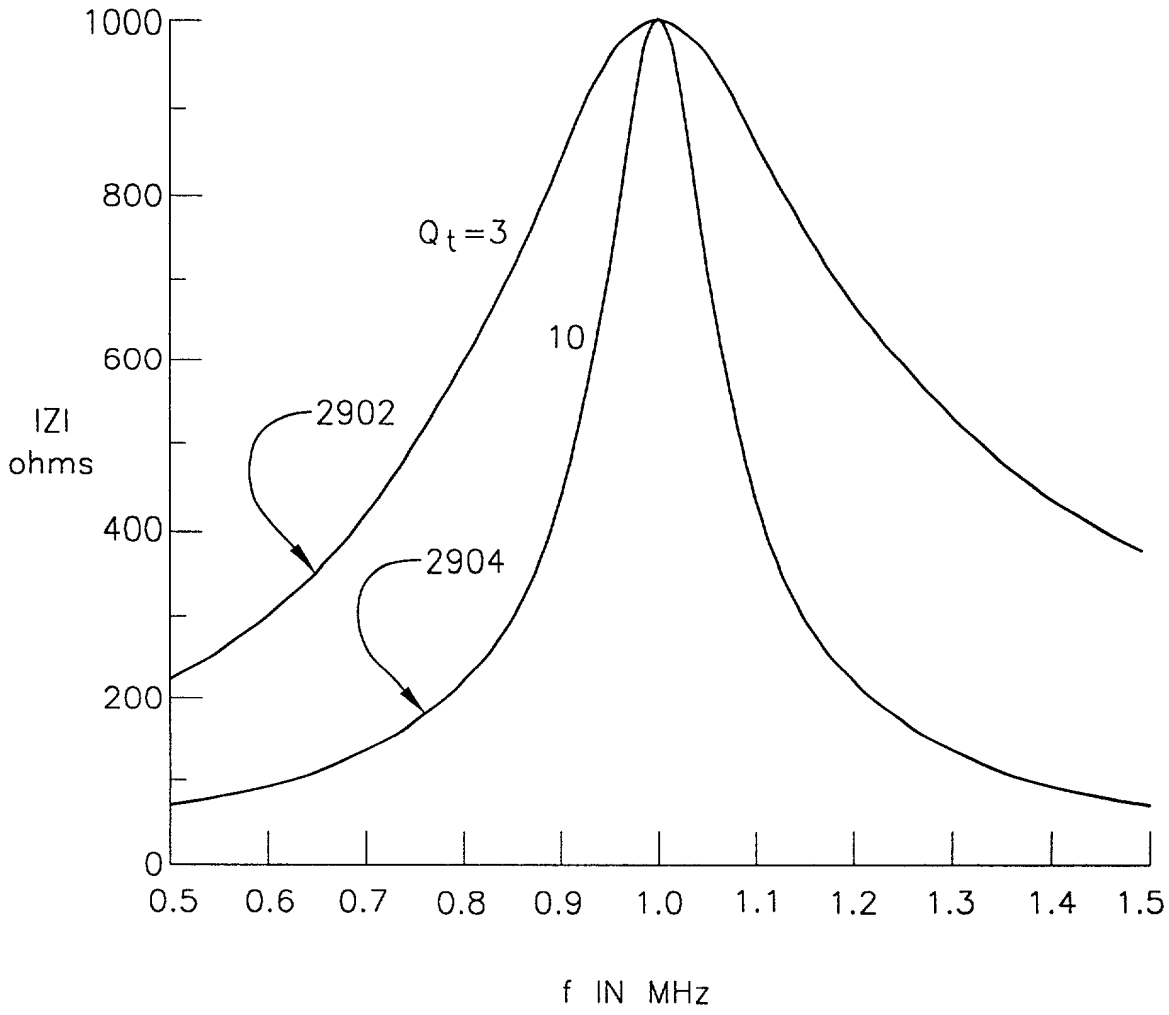

1000
800
600
400
200
0
IZI
ohms
$Q_t=3$
10
2902
2904
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
f IN MHz

FIG.30

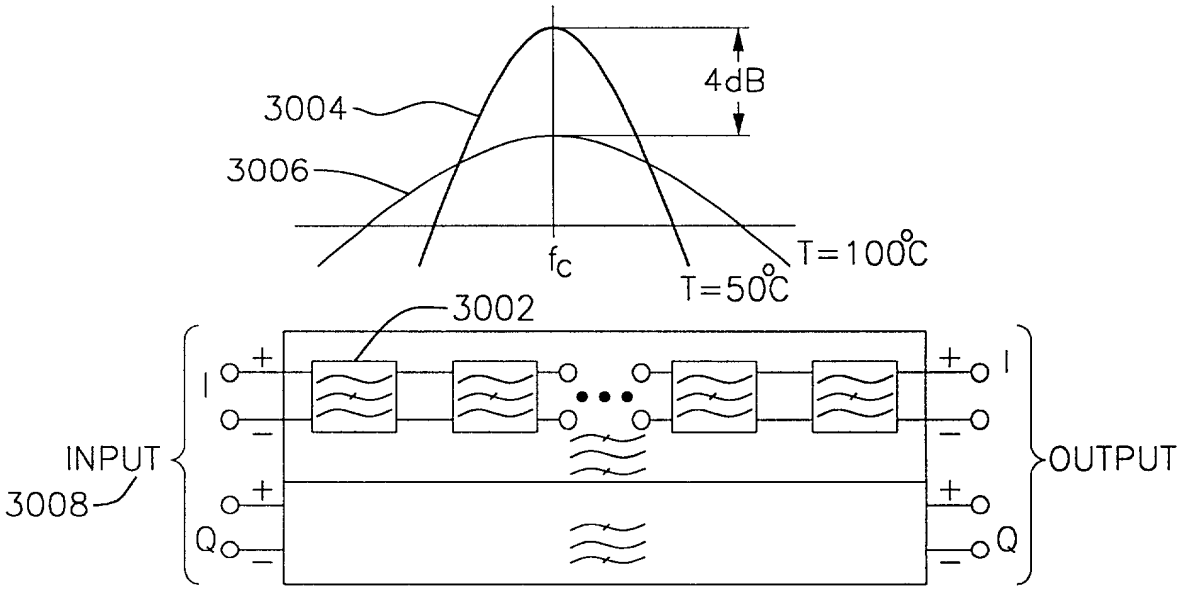


FIG.31a

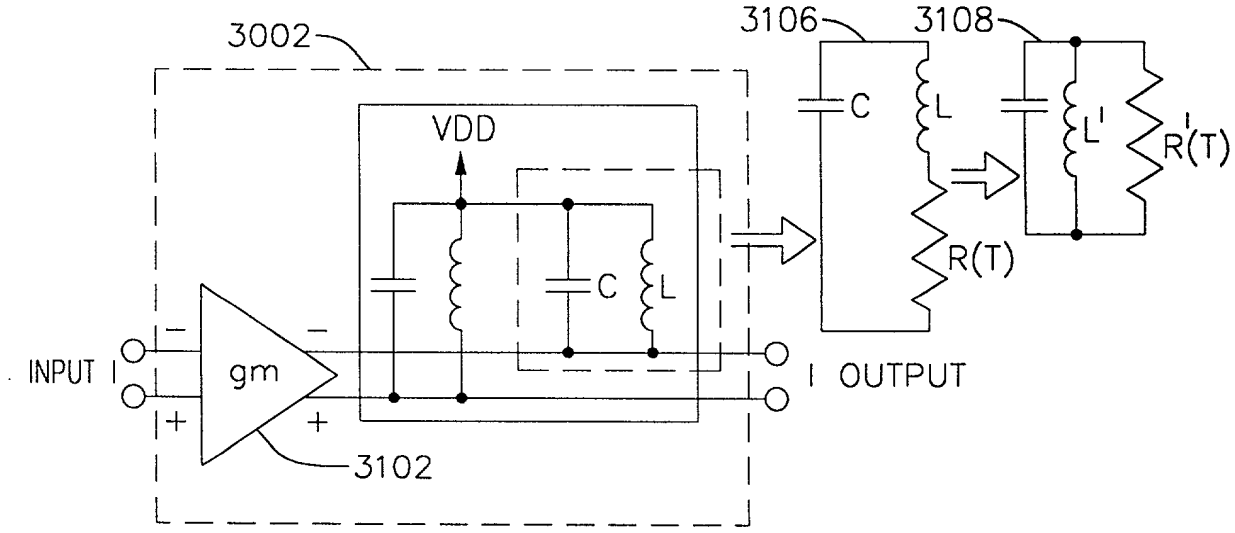


FIG. 31b

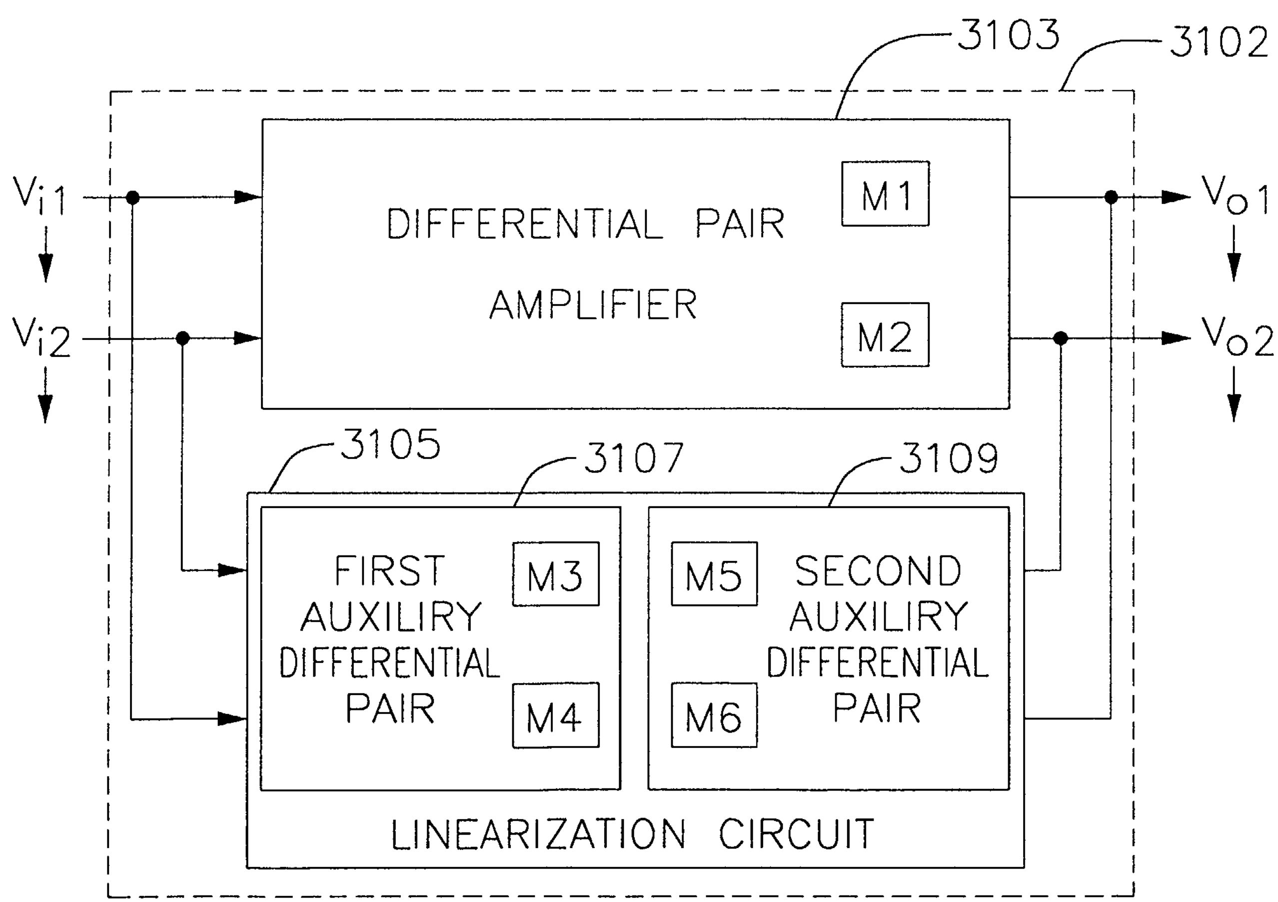

3103
3102
V_{i1}
V_{i2}
DIFFERENTIAL PAIR
AMPLIFIER
M1
M2
V_{o1}
V_{o2}
3105
3107
3109
FIRST
AUXILIRY
DIFFERENTIAL
PAIR
M3
M4
M5
M6
SECOND
AUXILIRY
DIFFERENTIAL
PAIR
LINEARIZATION CIRCUIT

FIG.31c

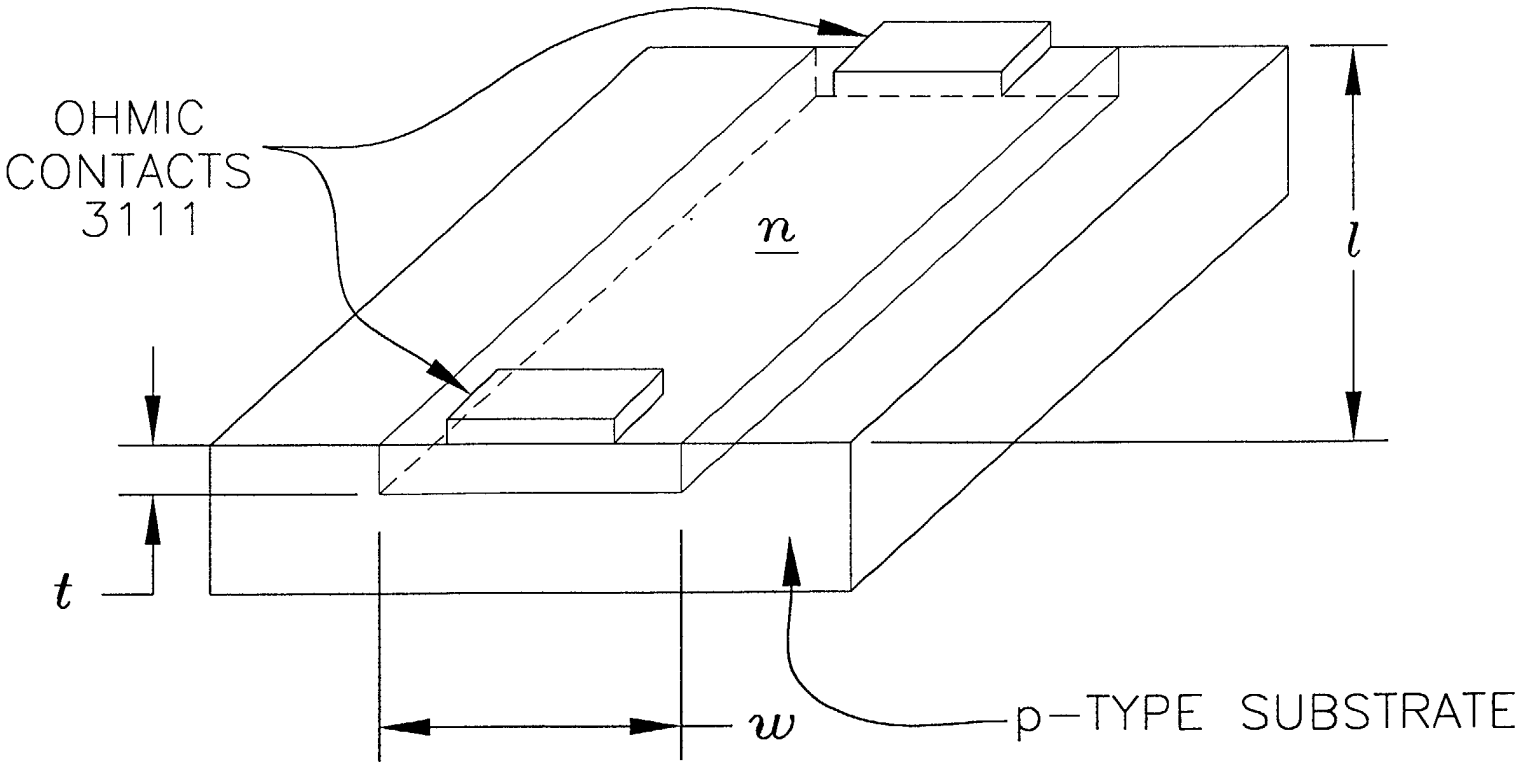


FIG.31d

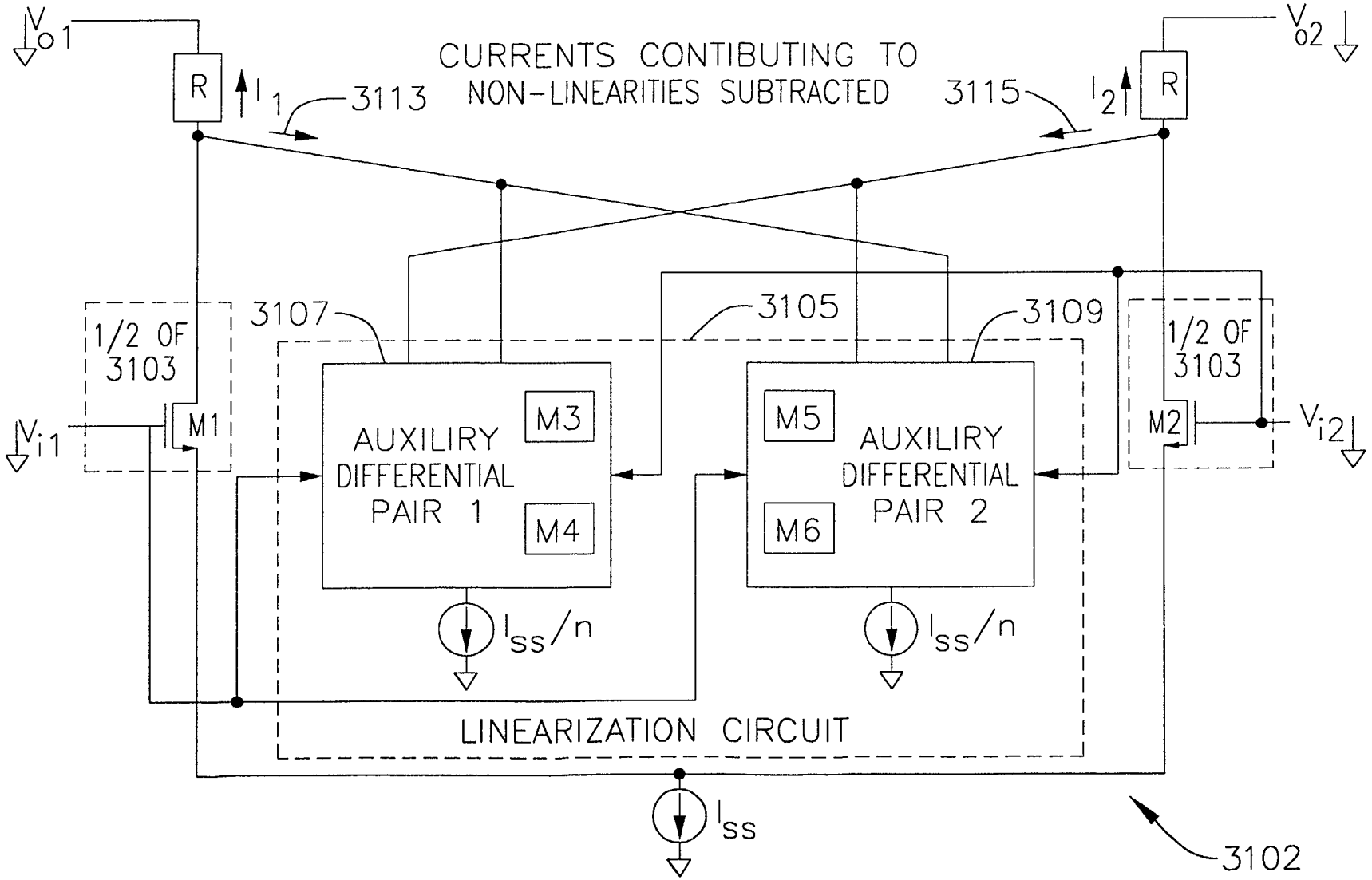

CURRENTS CONTIBUTING TO
NON-LINEARITIES SUBTRACTED
V_{o1}
V_{o2}
R
R
I_1
I_2
3113
3115
3107
3105
3109
1/2 OF 3103
1/2 OF 3103
M1
M2
V_{i1}
V_{i2}
AUXILIRY DIFFERENTIAL PAIR 1
M3
M4
AUXILIRY DIFFERENTIAL PAIR 2
M5
M6
I_{ss}/n
I_{ss}/n
LINEARIZATION CIRCUIT
I_{ss}
3102

FIG.31e

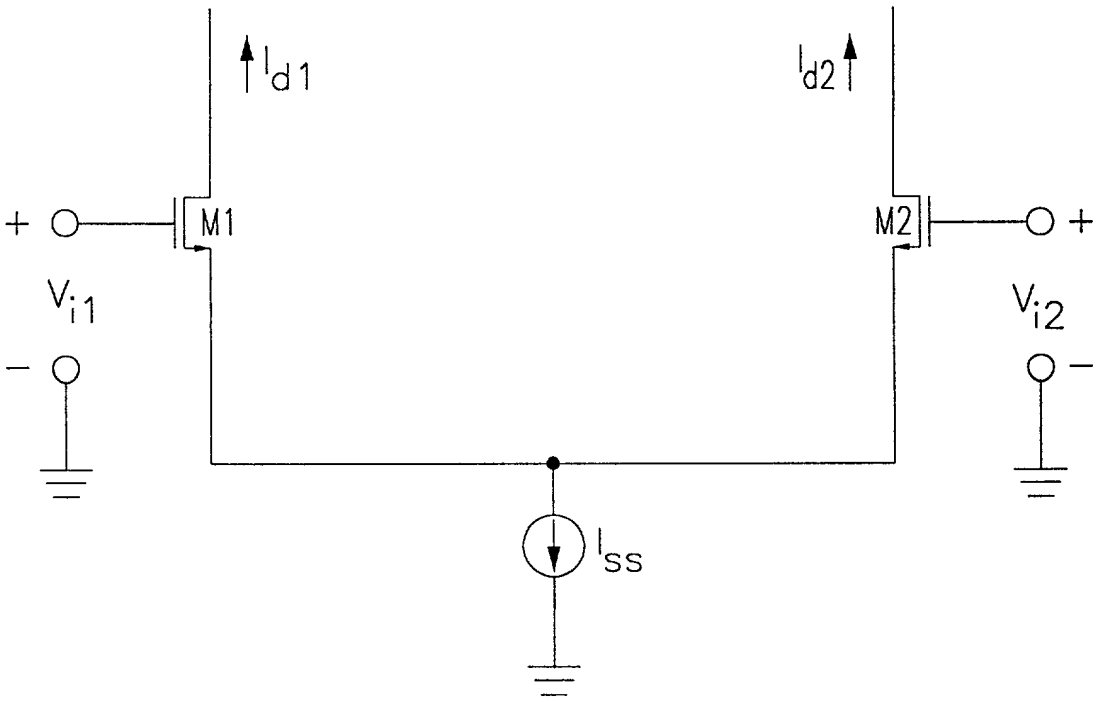


FIG.31f

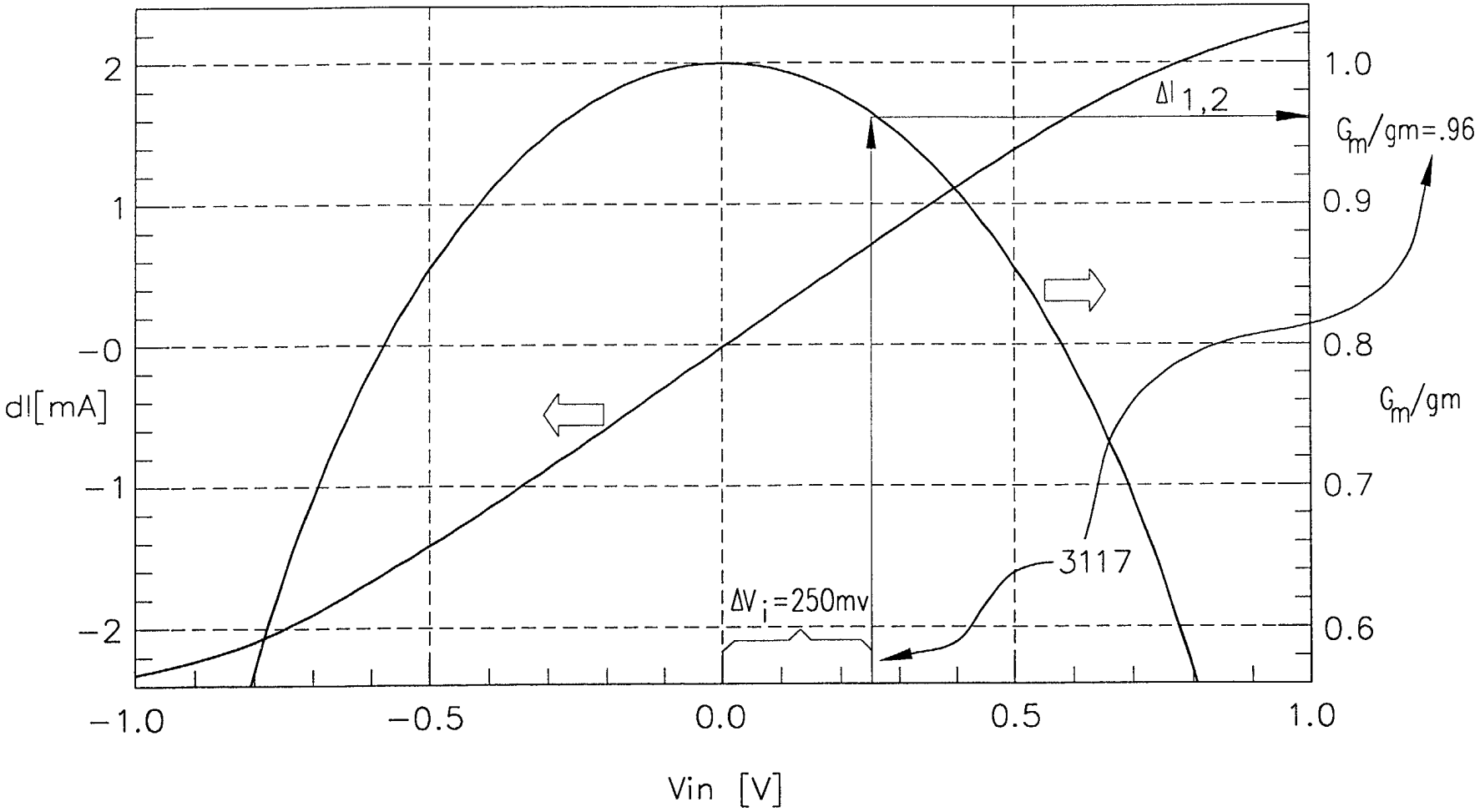
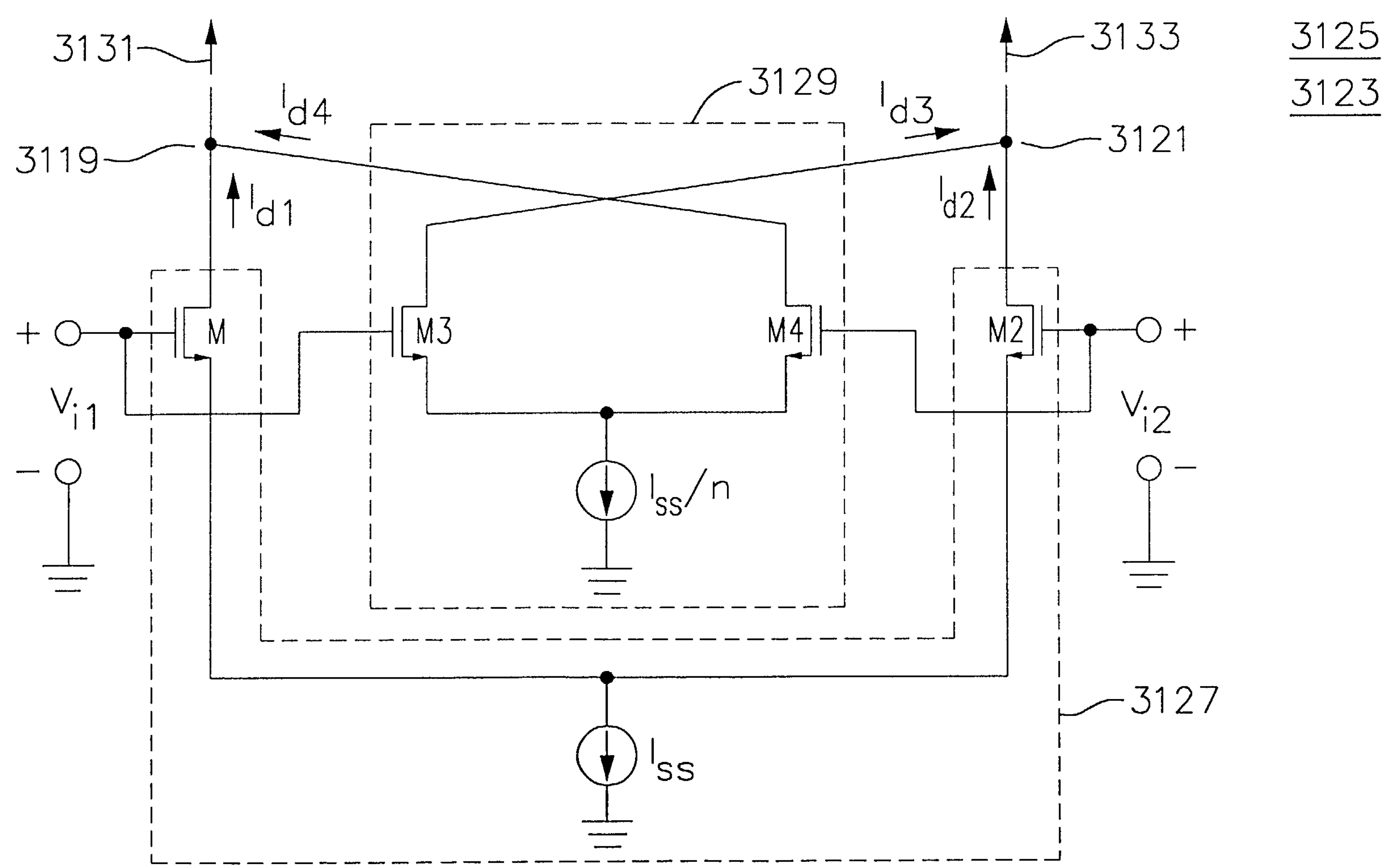
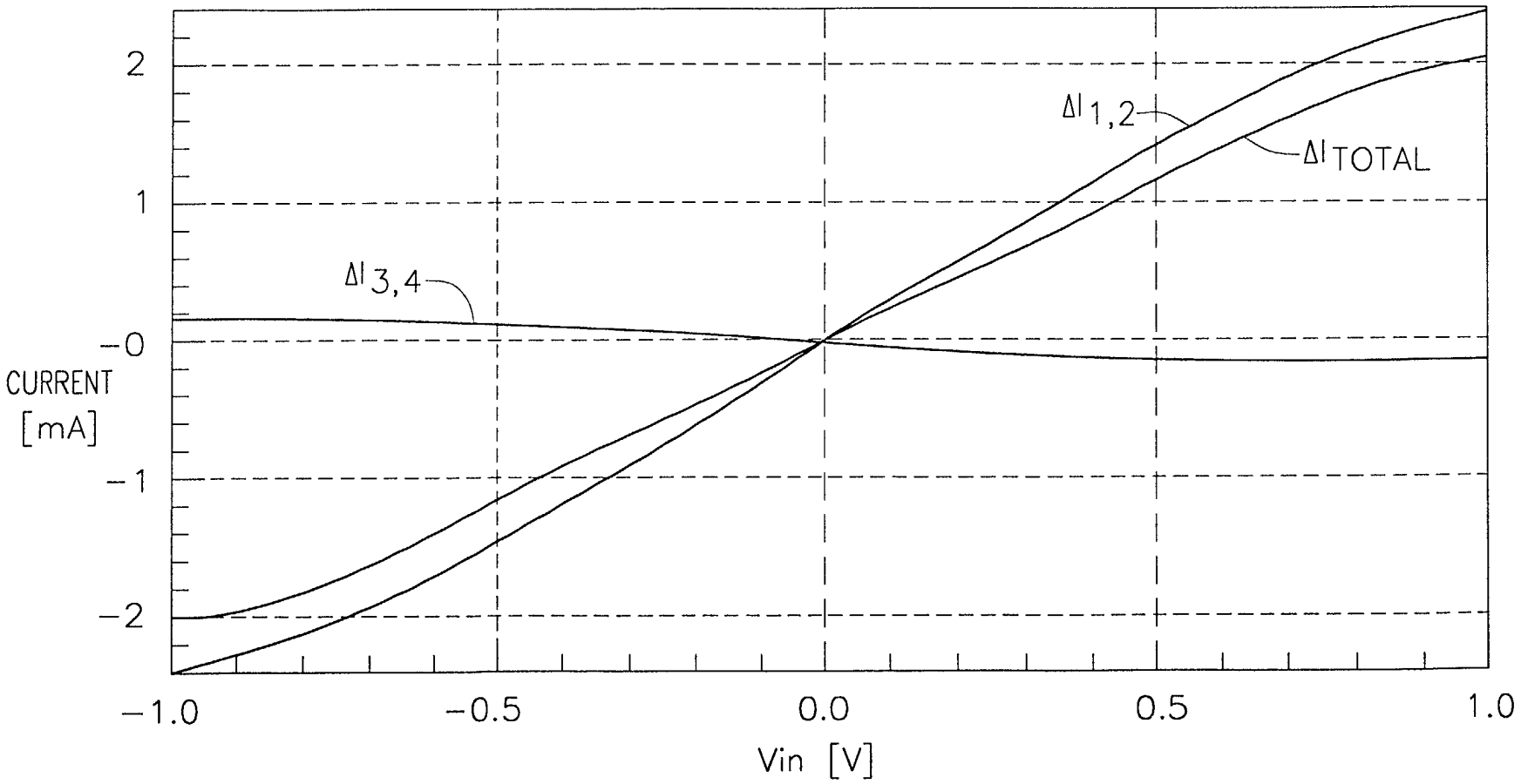


FIG. 31g



3131
3133
3125
3123
3129
3119
3121
I_{d4}
I_{d3}
I_{d1}
I_{d2}
M
M3
M4
M2
+
−
V_{i1}
V_{i2}
I_{ss}/n
I_{ss}
3127

FIG.31h



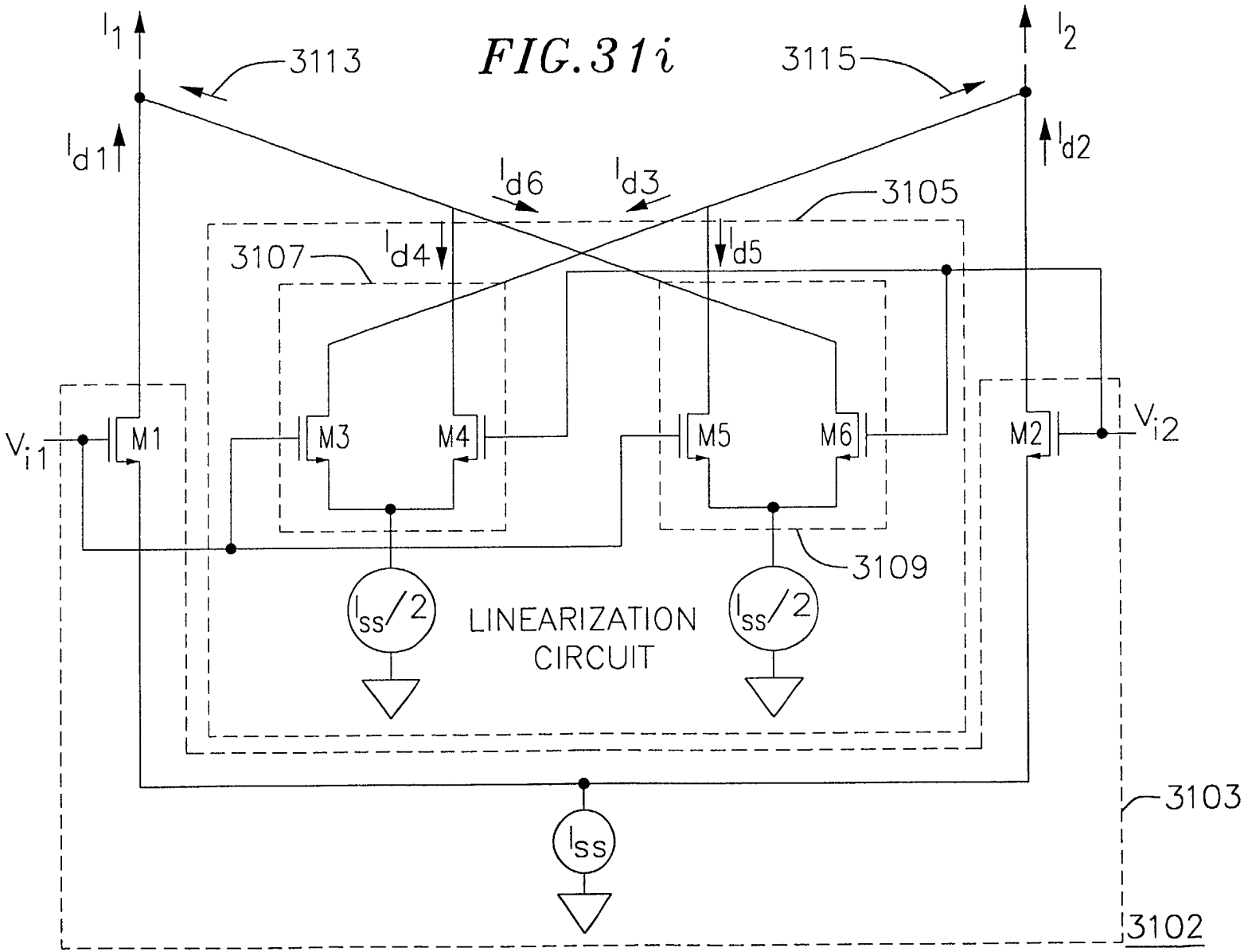


FIG. 31i

FIG.31j

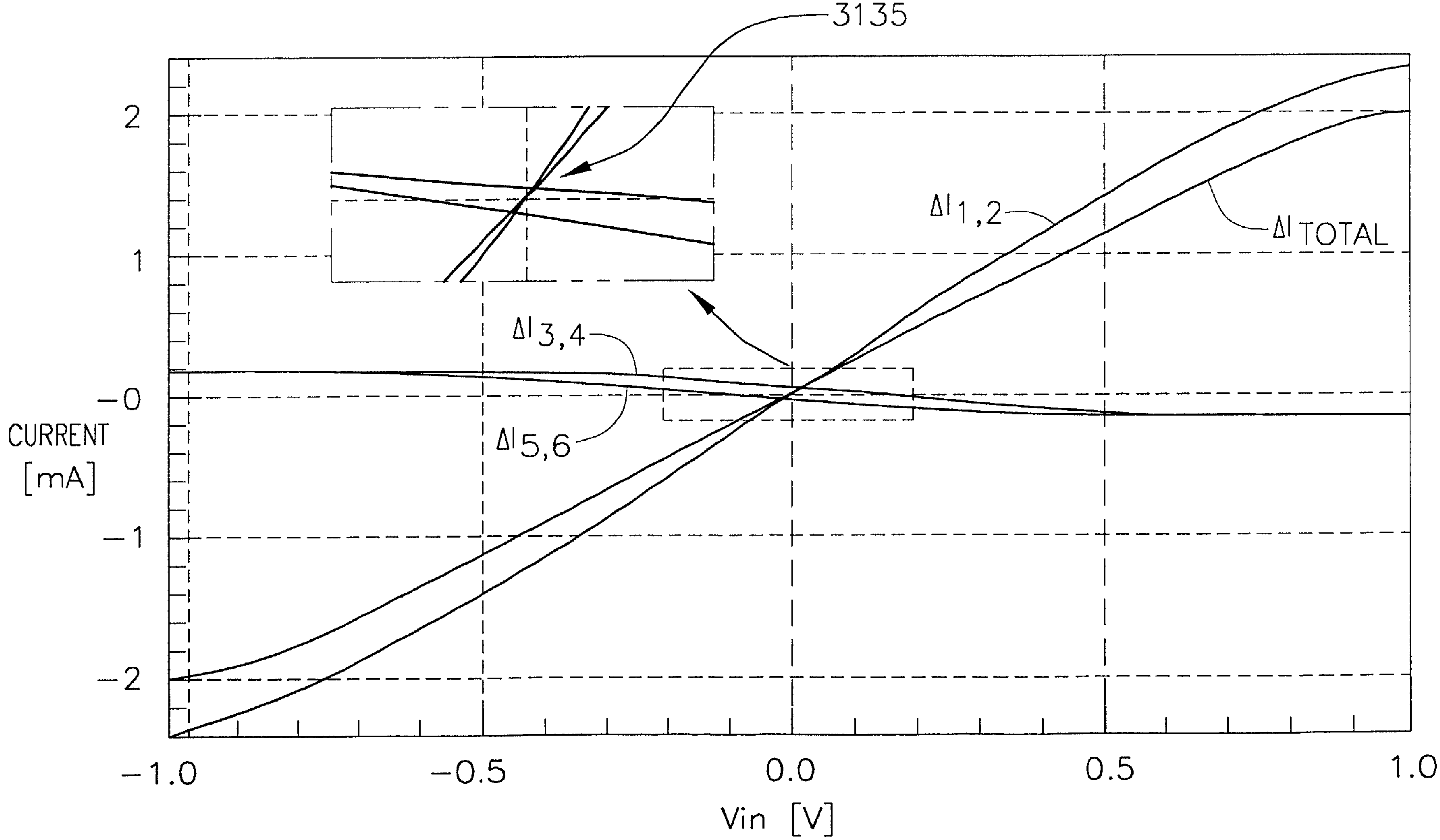
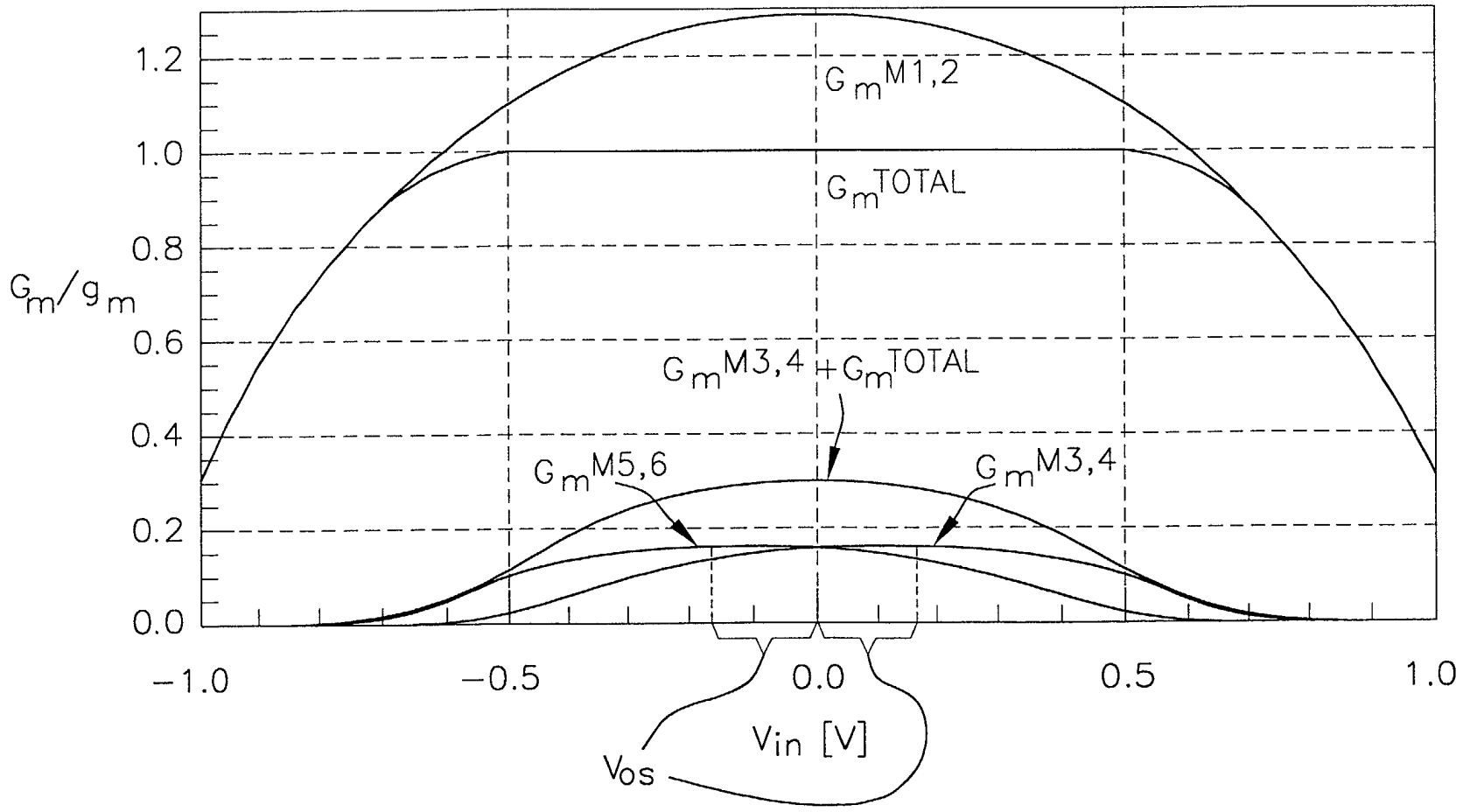
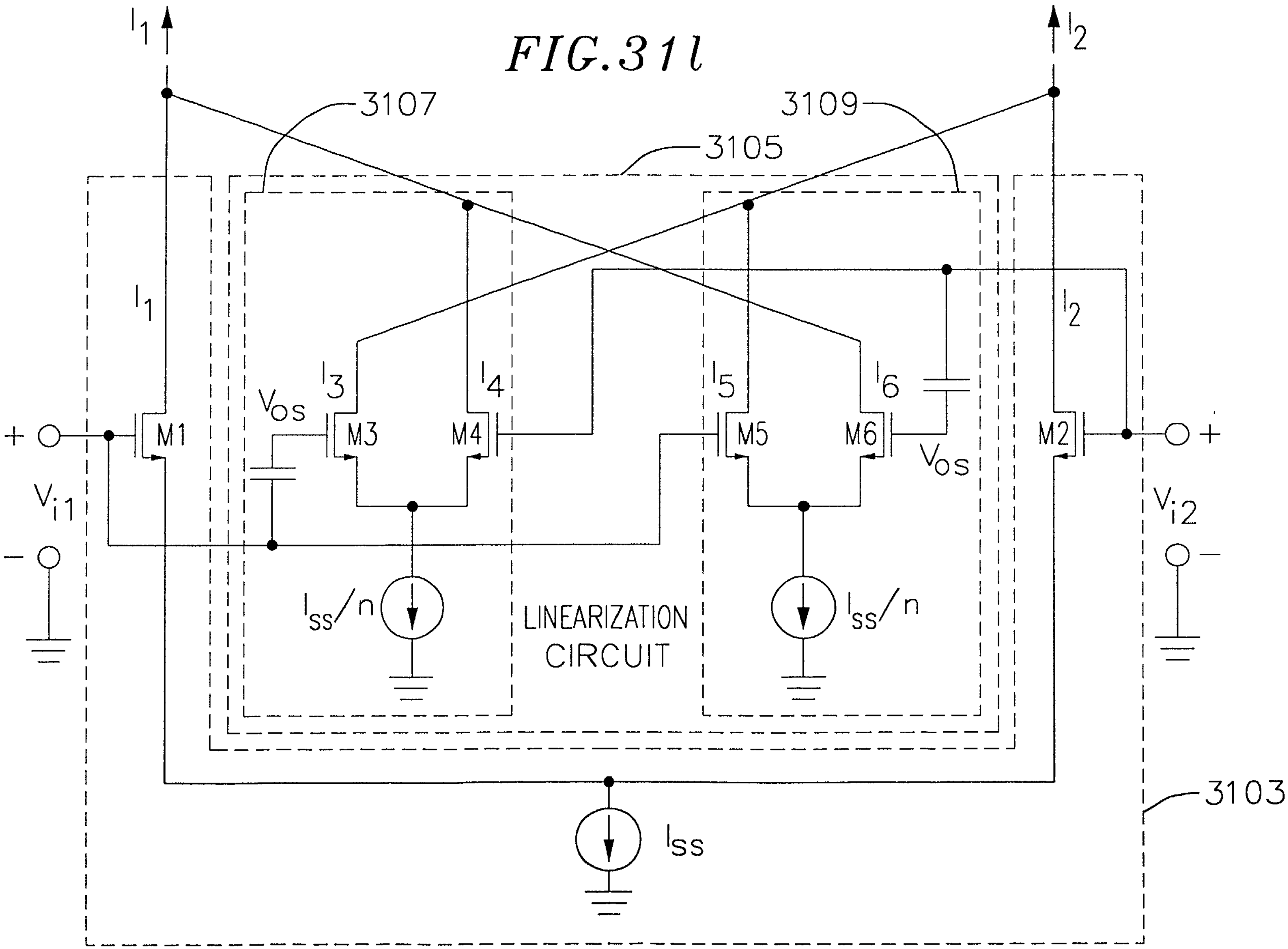

3135
ΔI 1,2
ΔI TOTAL
ΔI 3,4
ΔI 5,6
CURRENT
[mA]
2
1
−0
−1
−2
−1.0
−0.5
0.0
0.5
1.0
Vin [V]

FIG. 31k


1.2
1.0
0.8
0.6
0.4
0.2
0.0
G_m/g_m
$G_mM1,2$
G_mTOTAL
$G_mM3,4 + G_mTOTAL$
$G_mM5,6$
$G_mM3,4$
−1.0
−0.5
0.0
0.5
1.0
Vin [V]
Vos



I1
I2
3107
3109
3105
I1
I2
I3
I4
I5
I6
VOS
VOS
M1
M2
M3
M4
M5
M6
+
−
Vi1
+
−
Vi2
ISS/n
ISS/n
LINEARIZATION
CIRCUIT
ISS
3103

FIG.31l

FIG.31m

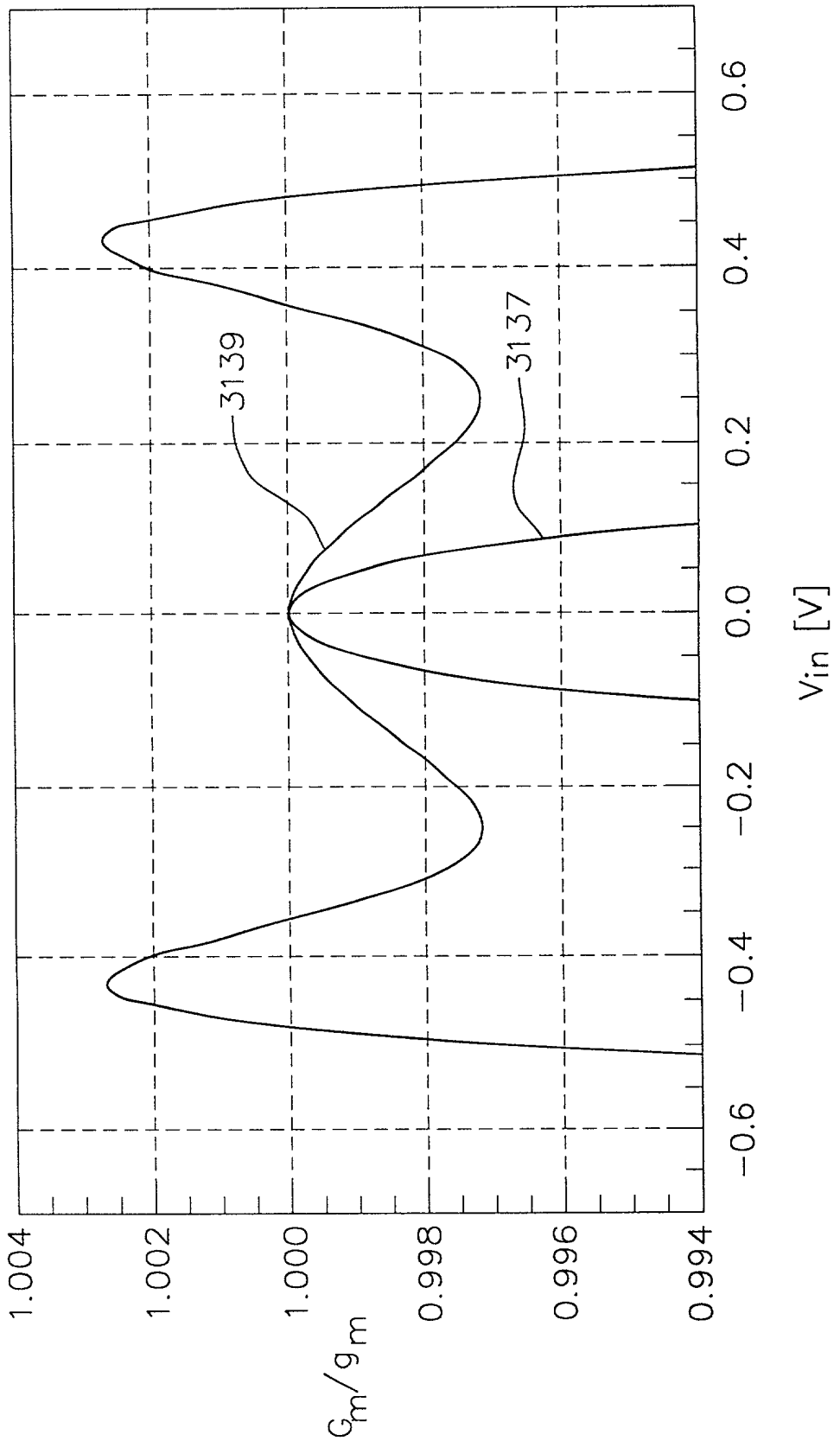
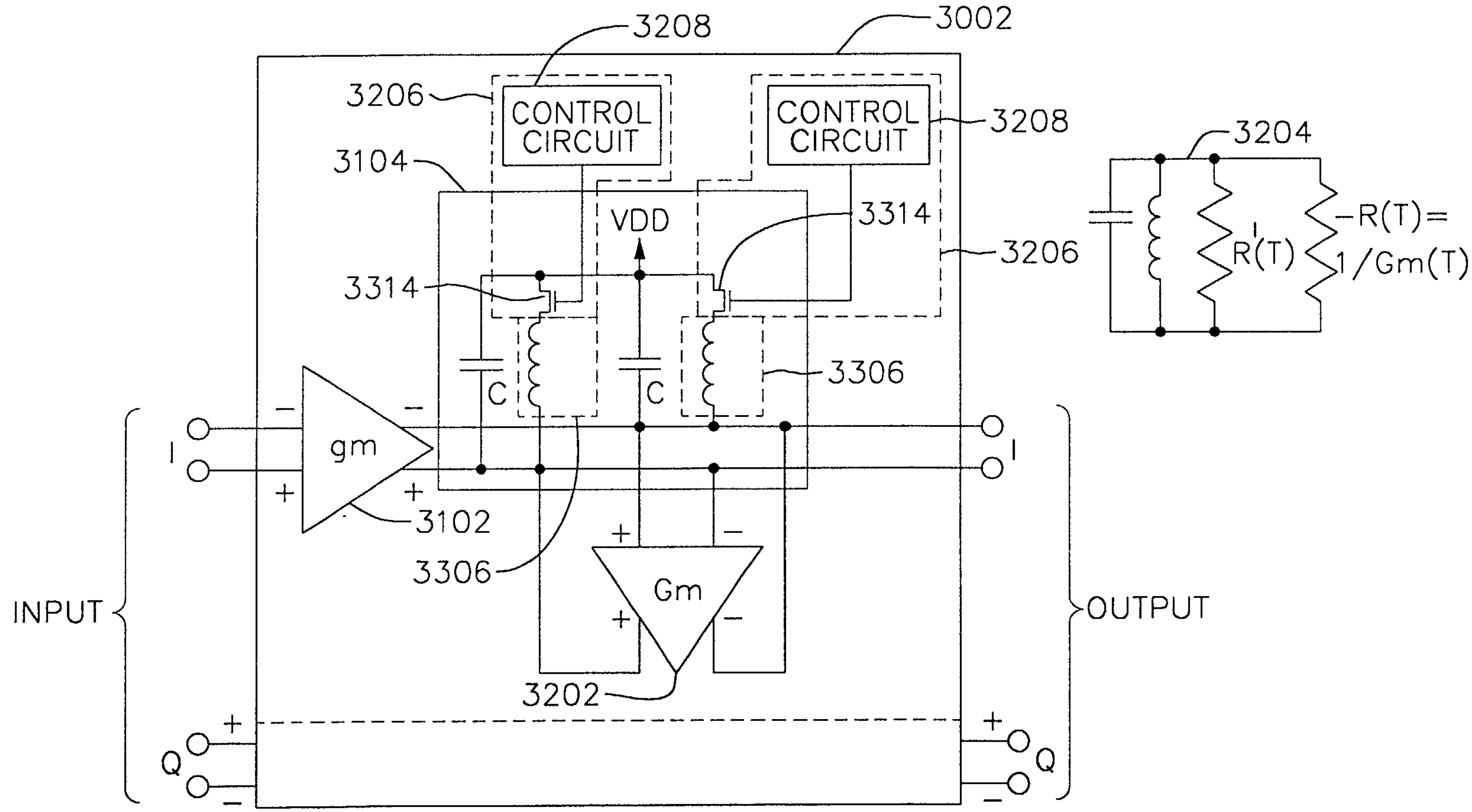

1.004
1.002
1.000
0.998
0.996
0.994
G_m/g_m
−0.6
−0.4
−0.2
0.0
0.2
0.4
0.6
V_{in} [V]
3139
3137

FIG.32



3208
3002
3206
CONTROL CIRCUIT
CONTROL CIRCUIT
3208
3204
3104
3314
VDD
3206
3314
R'(T)
-R(T)=
1/Gm(T)
C
C
3306
gm
I
I
3102
3306
Gm
INPUT
OUTPUT
3202
Q
Q

FIG.33

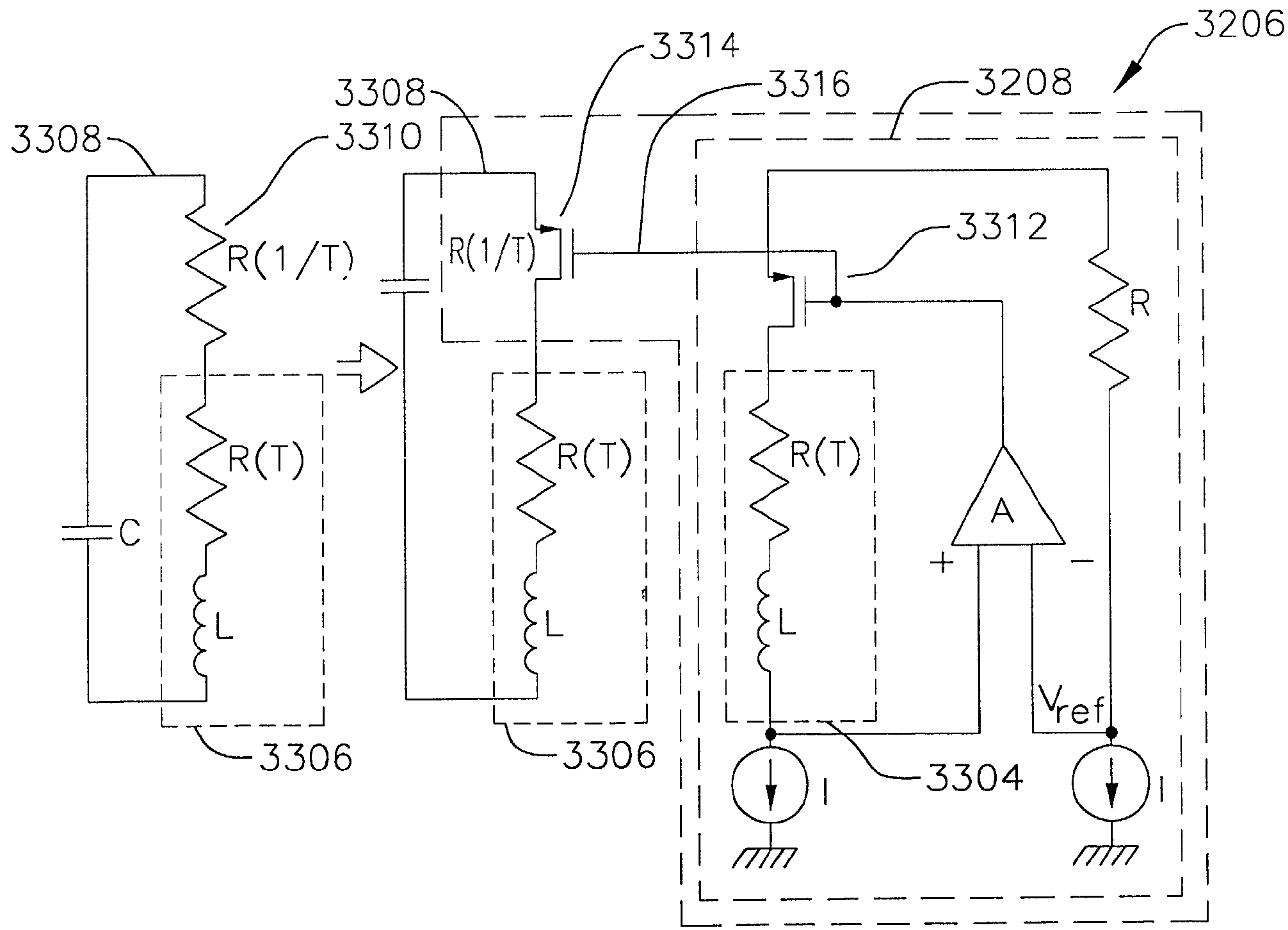

3206
3208
3308
3310
3308
3314
3316
3312
R(1/T)
R(1/T)
R(T)
R(T)
R(T)
L
L
L
C
R
A
+
−
V_{ref}
I
I
3306
3306
3304

FIG. 34

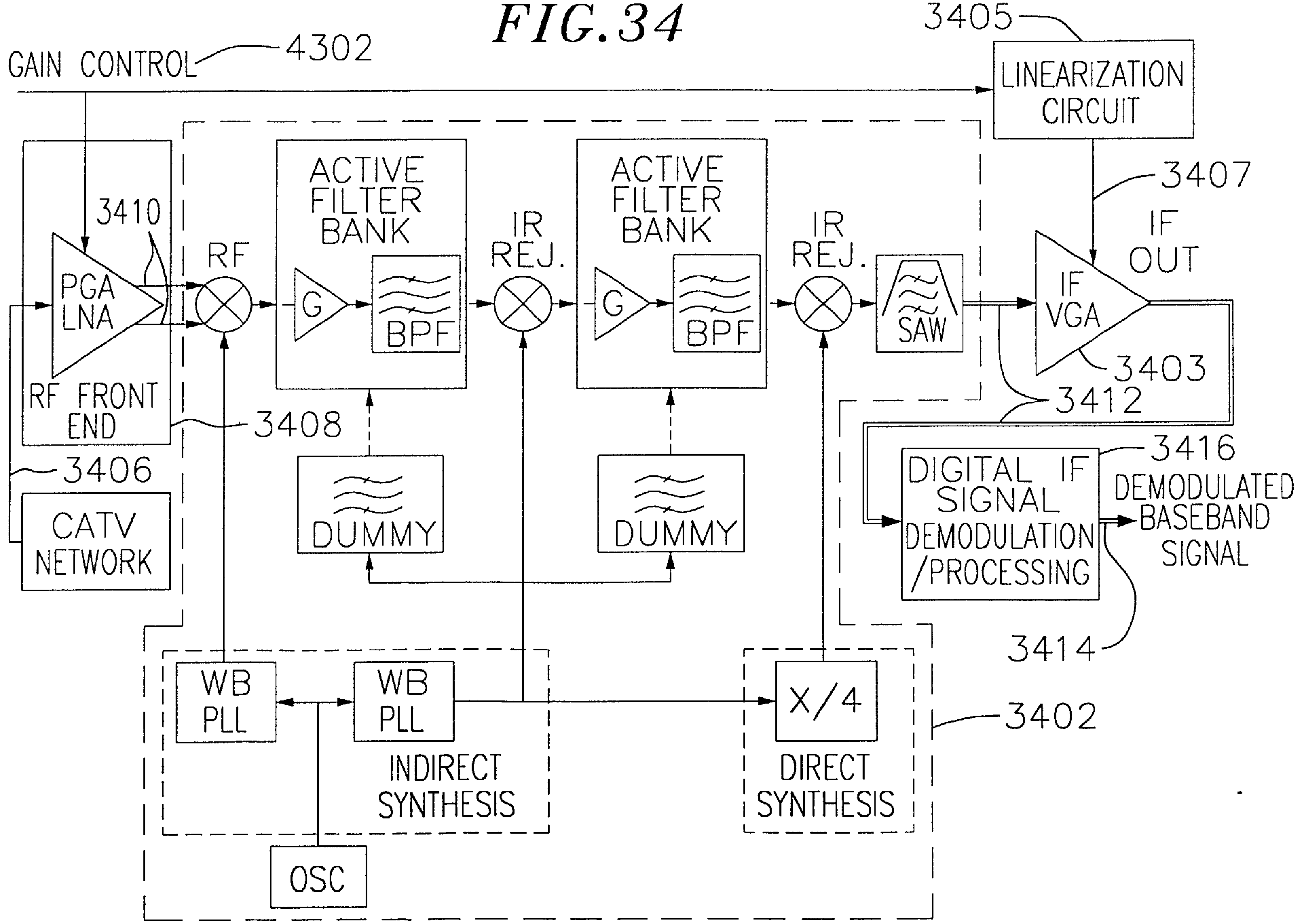

GAIN CONTROL
4302
3405
LINEARIZATION CIRCUIT
3407
IF OUT
IF VGA
3403
3412
3410
PGA LNA
RF FRONT END
3408
3406
CATV NETWORK
RF
ACTIVE FILTER BANK
G
BPF
IR REJ.
ACTIVE FILTER BANK
G
BPF
IR REJ.
SAW
DUMMY
DUMMY
DIGITAL IF SIGNAL DEMODULATION /PROCESSING
3416
DEMODULATED BASEBAND SIGNAL
3414
WB PLL
WB PLL
INDIRECT SYNTHESIS
OSC
X/4
DIRECT SYNTHESIS
3402

FIG.35

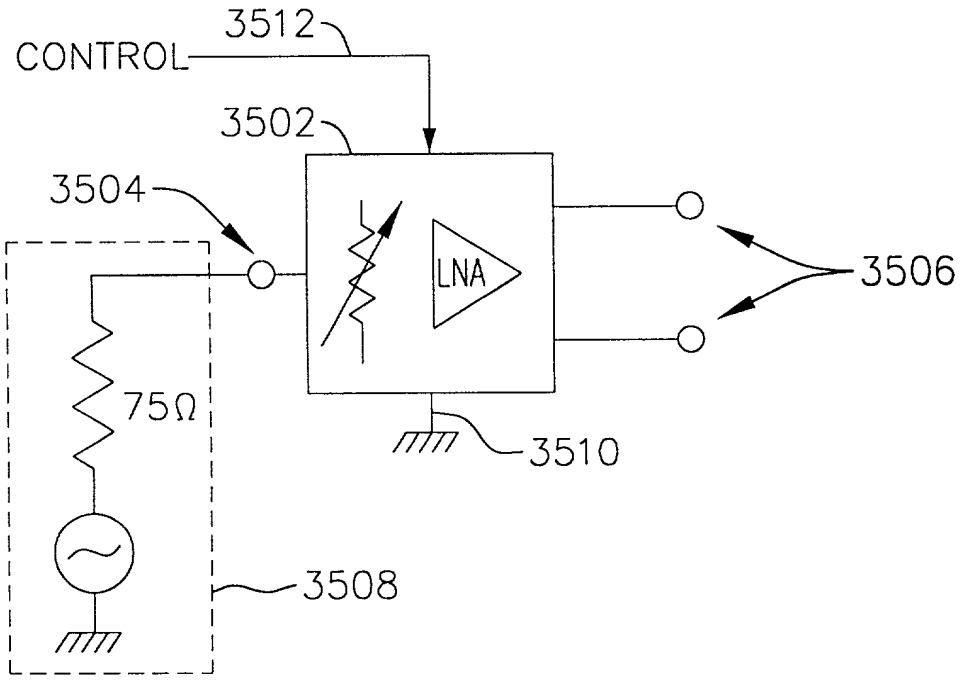


FIG. 36

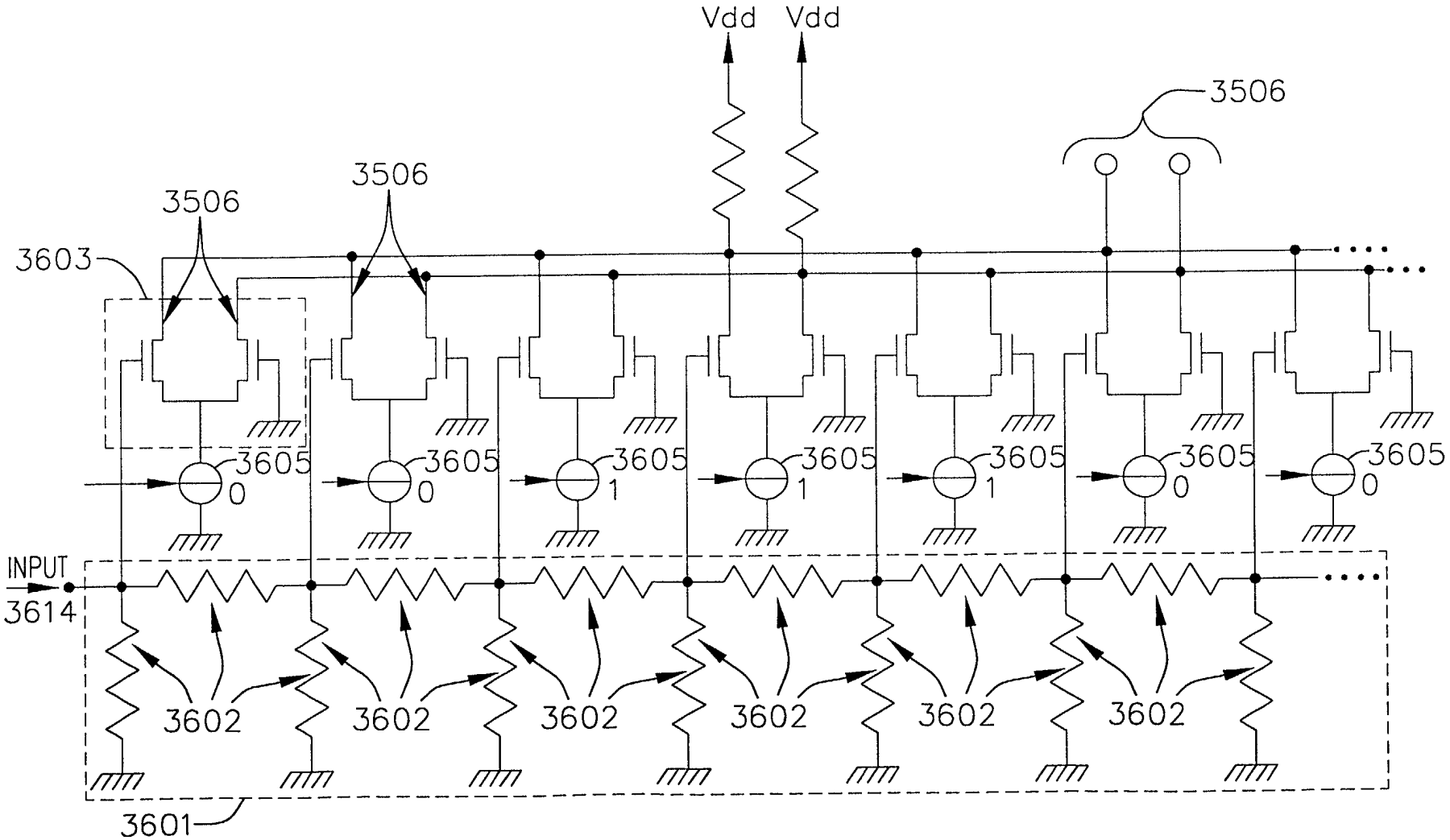

Vdd
Vdd
3506
3506
3506
3603
3605
0
3605
0
3605
1
3605
1
3605
1
3605
0
3605
0
INPUT
3614
3602
3602
3602
3602
3602
3602
3601

FIG.37

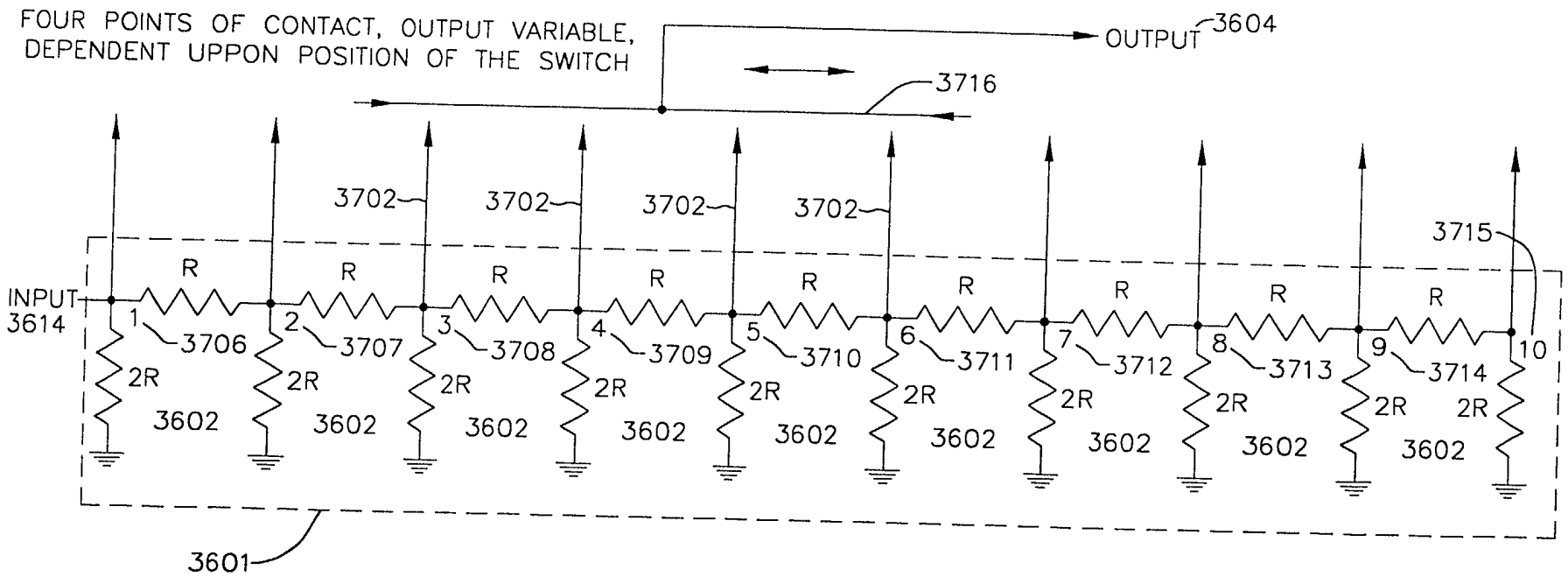

FOUR POINTS OF CONTACT, OUTPUT VARIABLE, DEPENDENT UPPON POSITION OF THE SWITCH
OUTPUT
3604
3716
3702
3715
INPUT
3614
R
2R
1
2
3
4
5
6
7
8
9
10
3706
3707
3708
3709
3710
3711
3712
3713
3714
3602
3601

FIG. 38

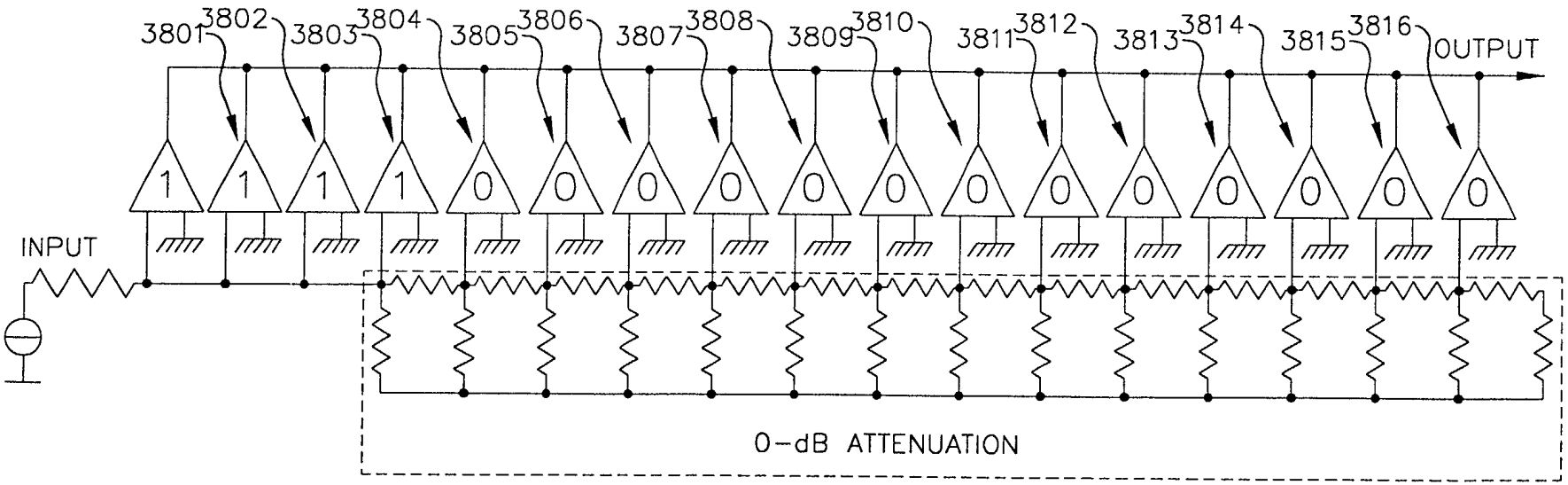

PGA SETTINGS
3801
3802
3803
3804
3805
3806
3807
3808
3809
3810
3811
3812
3813
3814
3815
3816
OUTPUT
1
1
1
1
0
0
0
0
0
0
0
0
0
0
0
0
INPUT
0-dB ATTENUATION

FIG.39

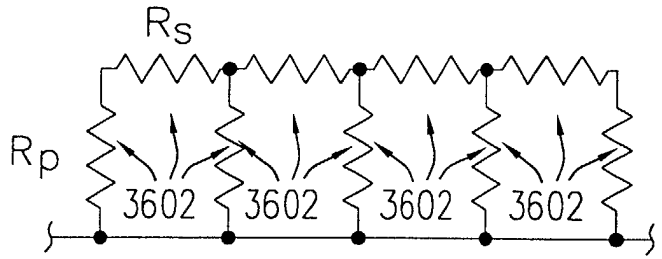

Rs
Rp
3602
3602
3602
3602

FIG.40

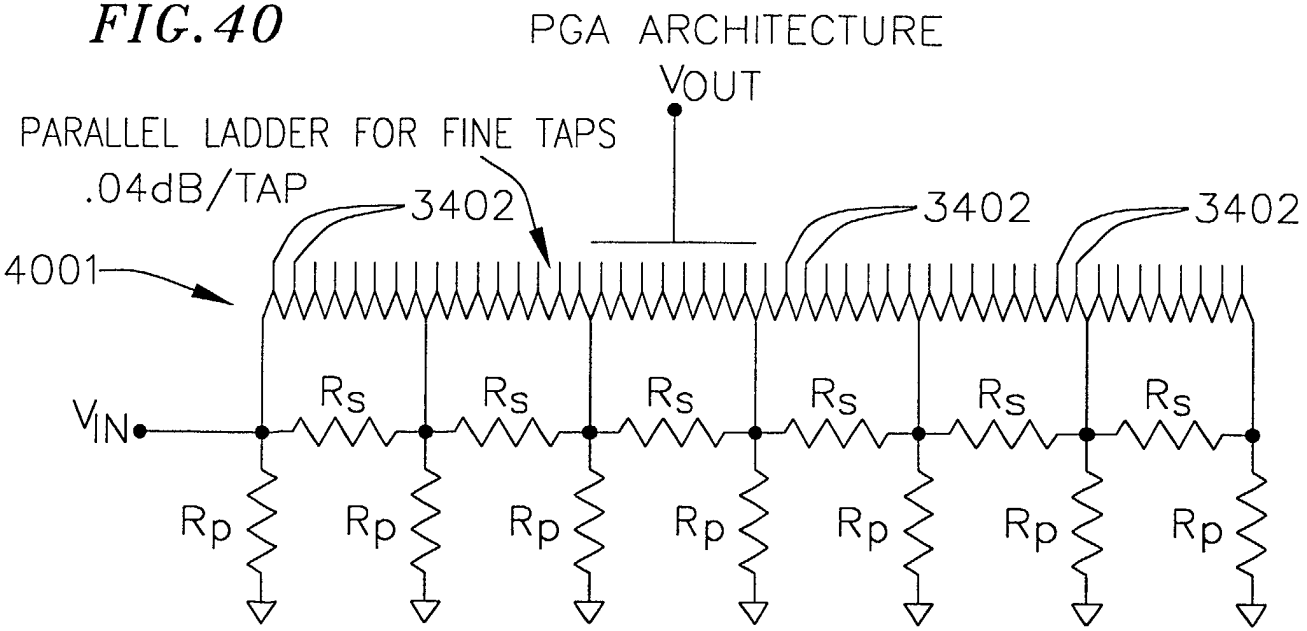

PGA ARCHITECTURE
VOUT
PARALLEL LADDER FOR FINE TAPS
.04dB/TAP
3402
3402
3402
4001
VIN
Rs
Rs
Rs
Rs
Rs
Rs
Rp
Rp
Rp
Rp
Rp
Rp
Rp

FIG.41

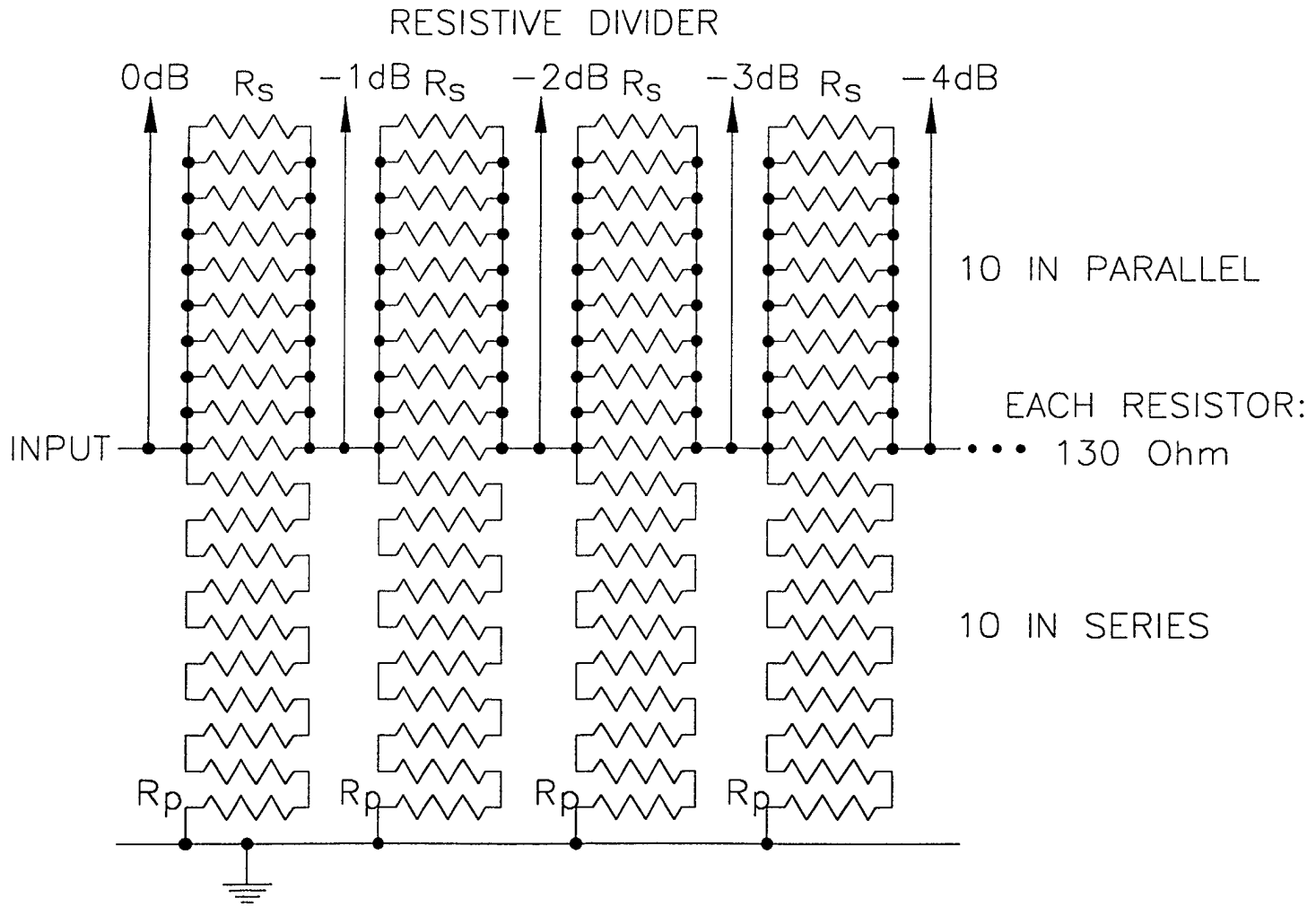


FIG. 42

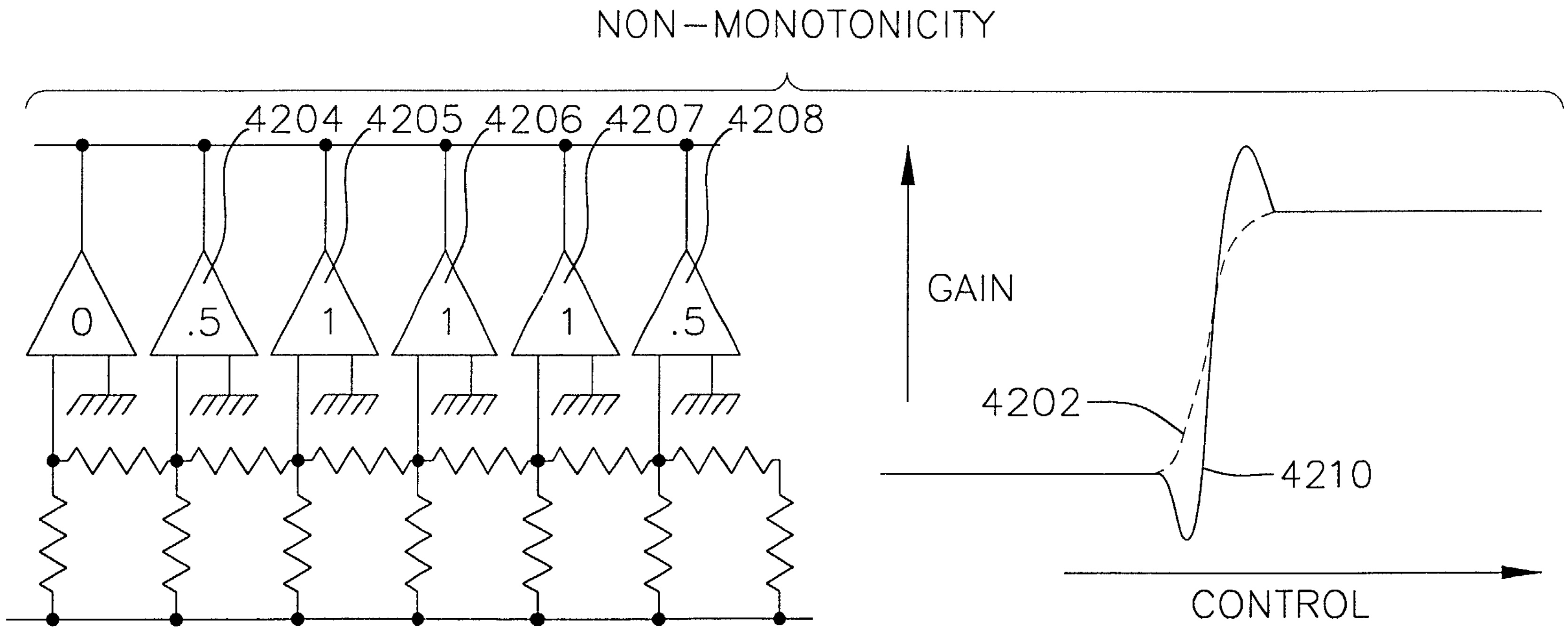

NON-MONOTONICITY
4204
4205
4206
4207
4208
0
.5
1
1
1
.5
GAIN
4202
4210
CONTROL

FIG. 43

CLAMPING CONTROL RANGE

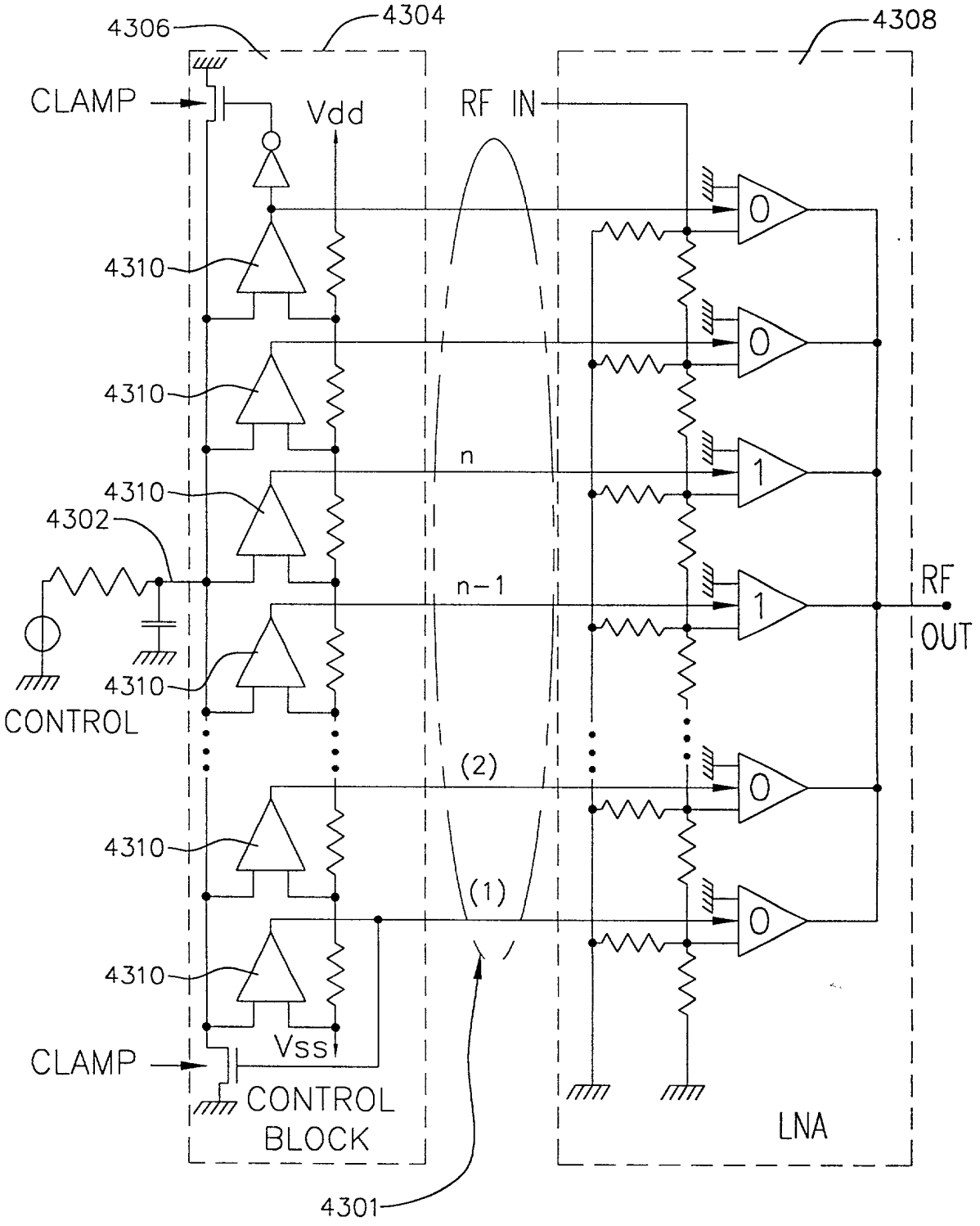


FIG.44a

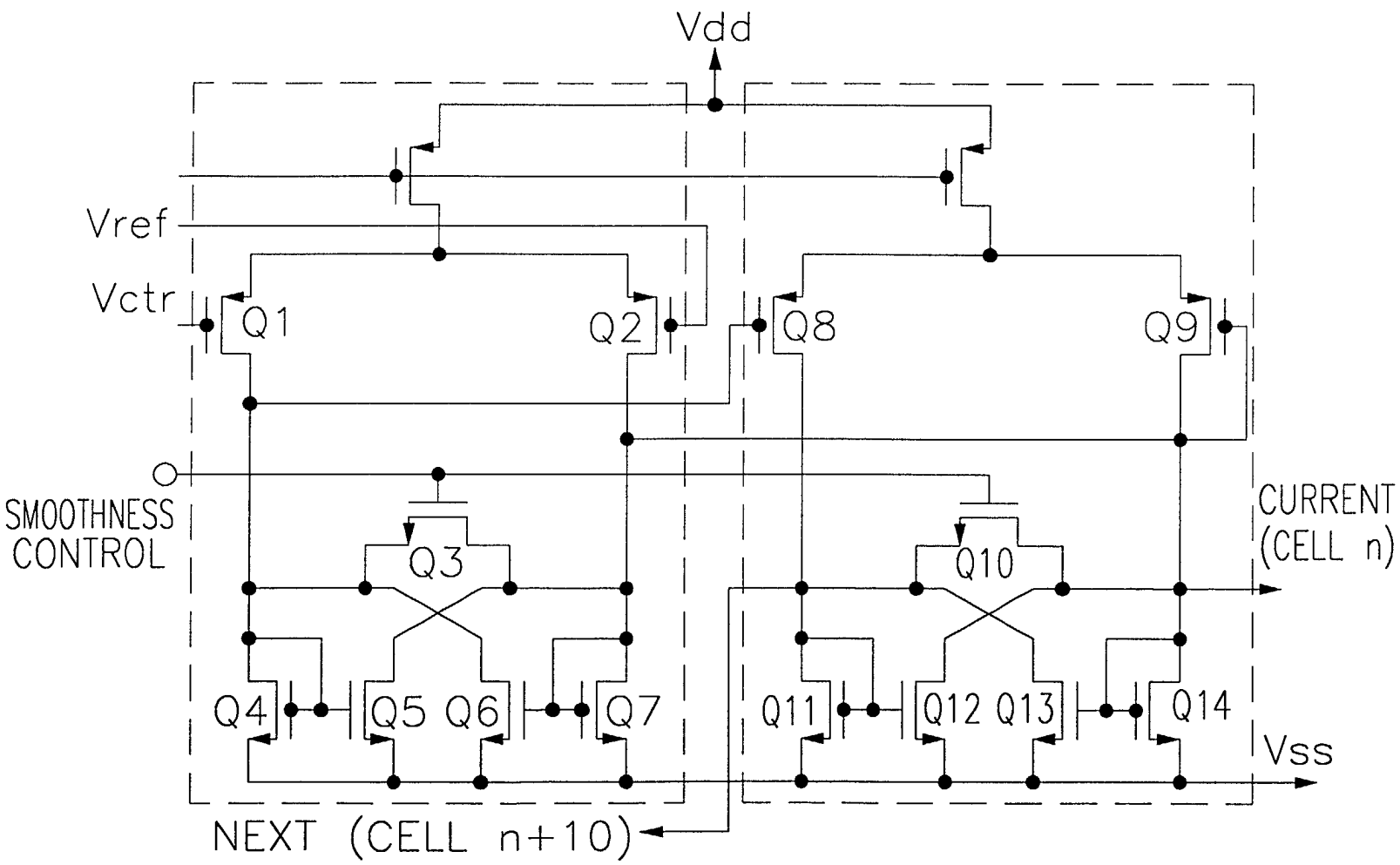

CONTROLLED GAIN COMPARATOR
Vdd
Vref
Vctr
Q1
Q2
Q8
Q9
SMOOTHNESS CONTROL
Q3
Q10
CURRENT (CELL n)
Q4
Q5 Q6
Q7
Q11
Q12 Q13
Q14
Vss
NEXT (CELL n+10)

FIG. 44b

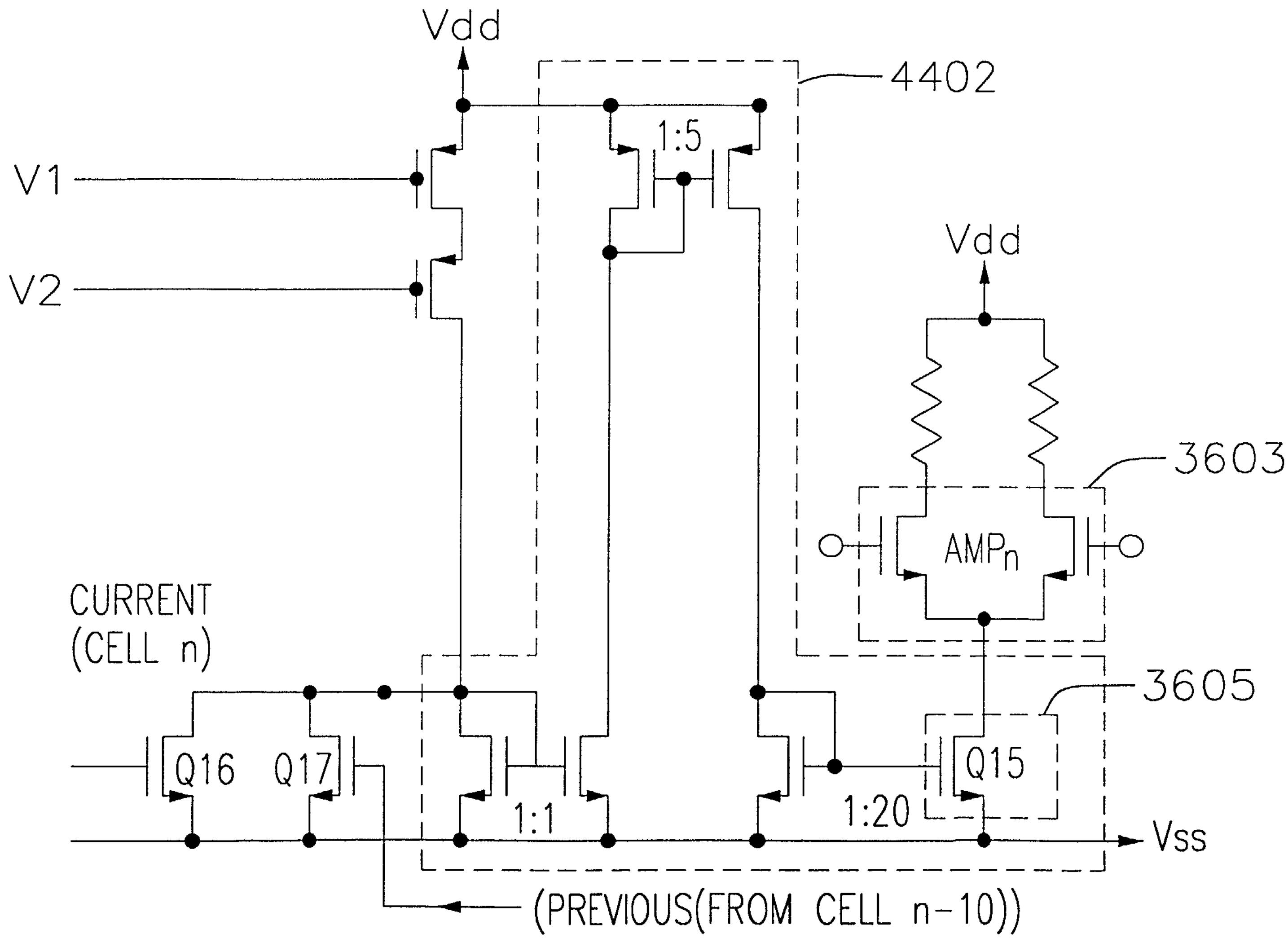


FIG. 45a

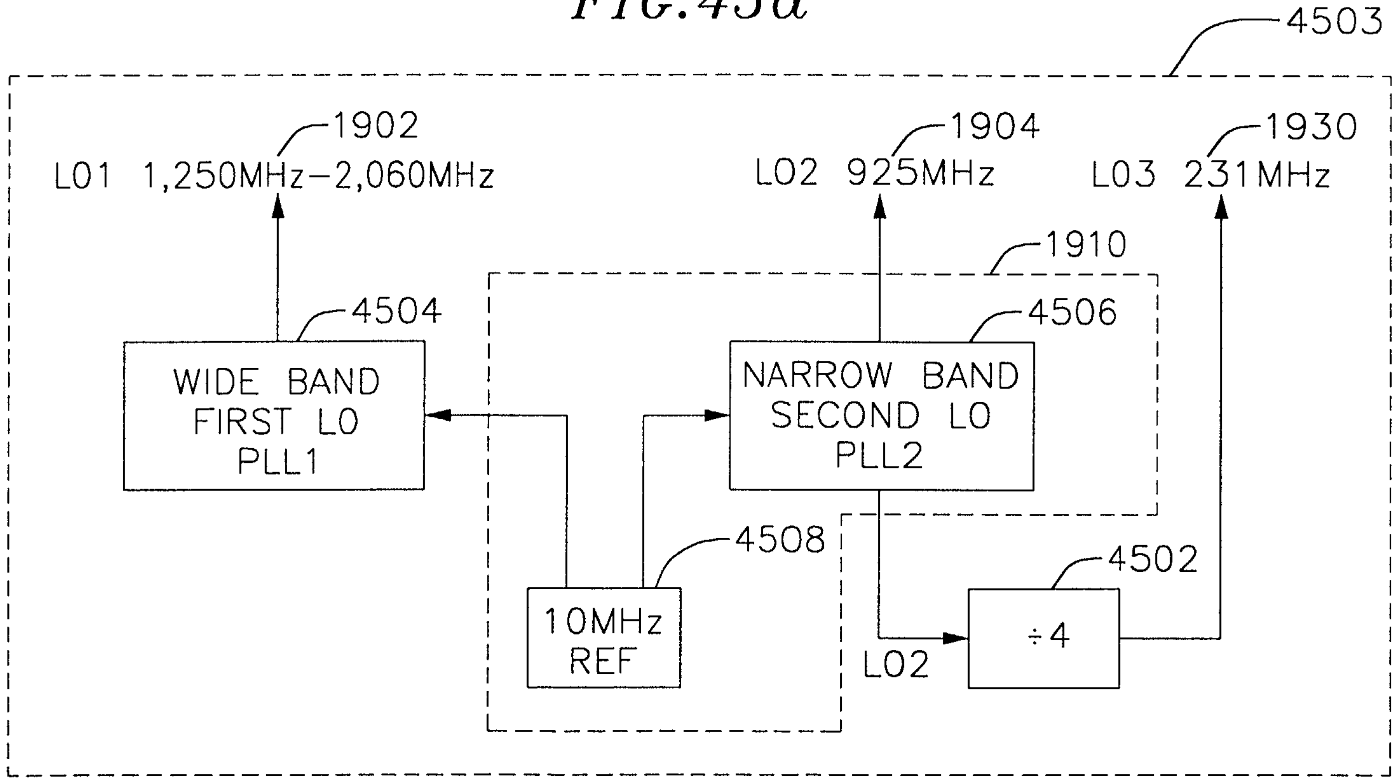

4503
1902
L01 1,250MHz–2,060MHz
1904
L02 925MHz
1930
L03 231MHz
1910
4504
WIDE BAND
FIRST L0
PLL1
4506
NARROW BAND
SECOND L0
PLL2
4508
10MHz
REF
4502
÷4
L02

FIG.45b

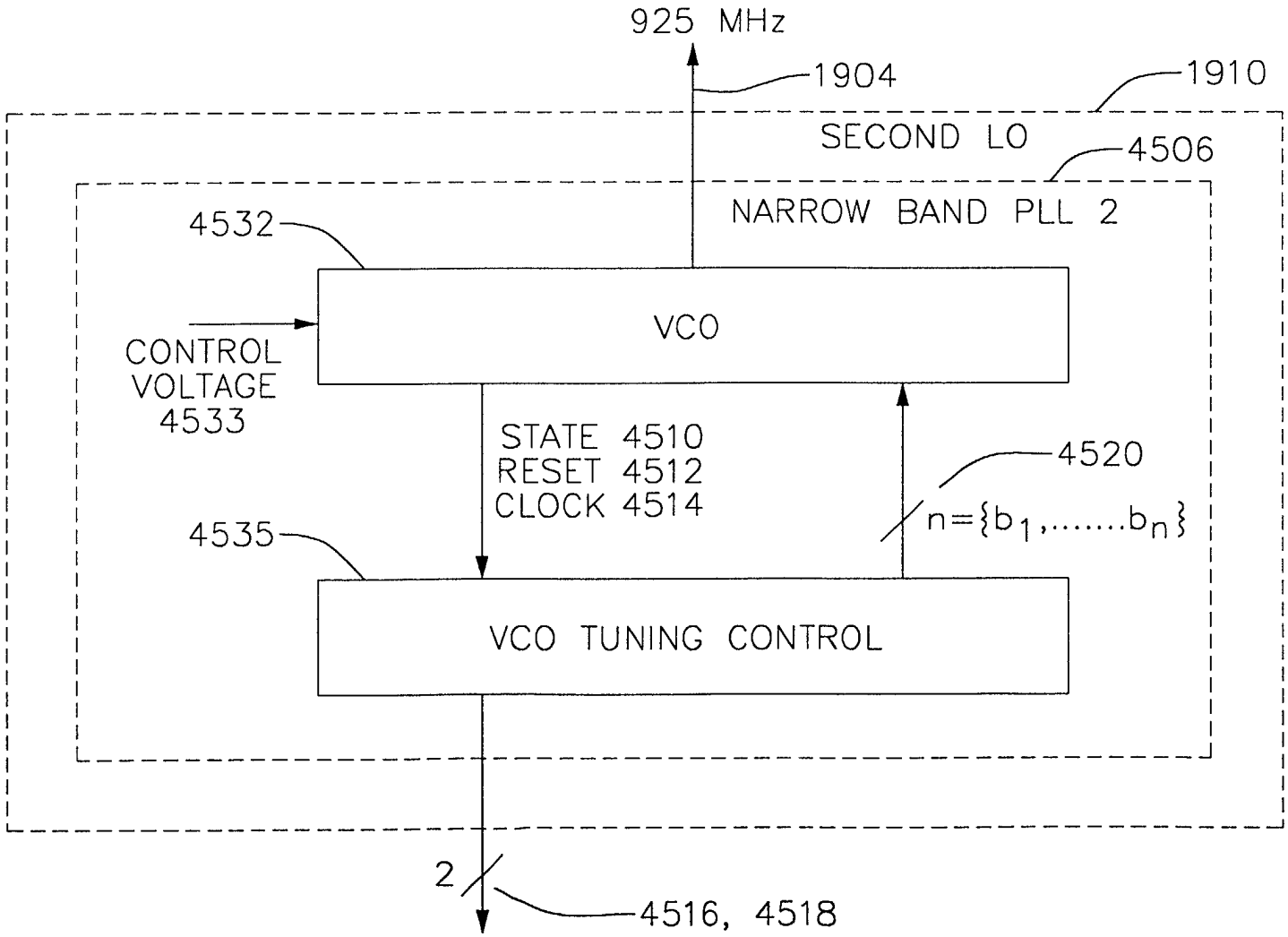


FIG. 45c

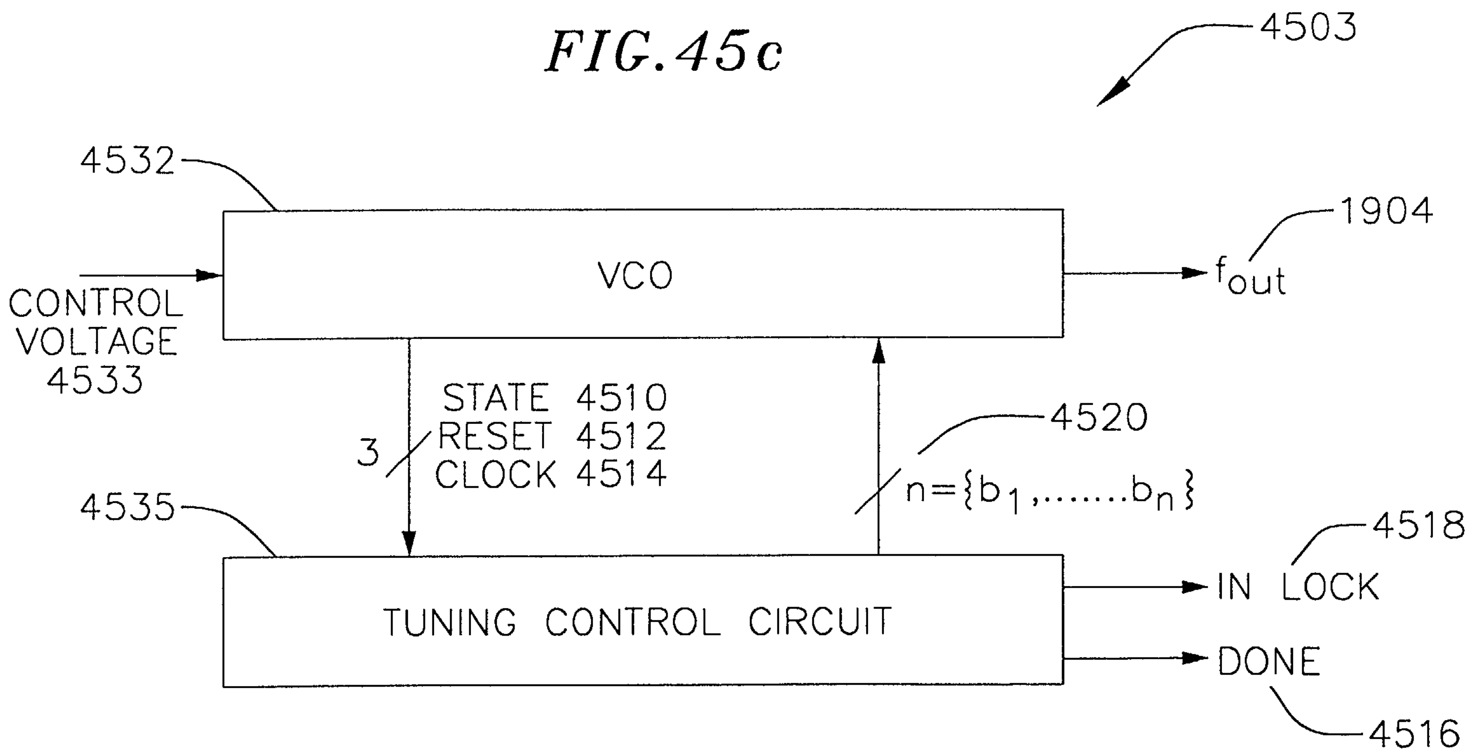
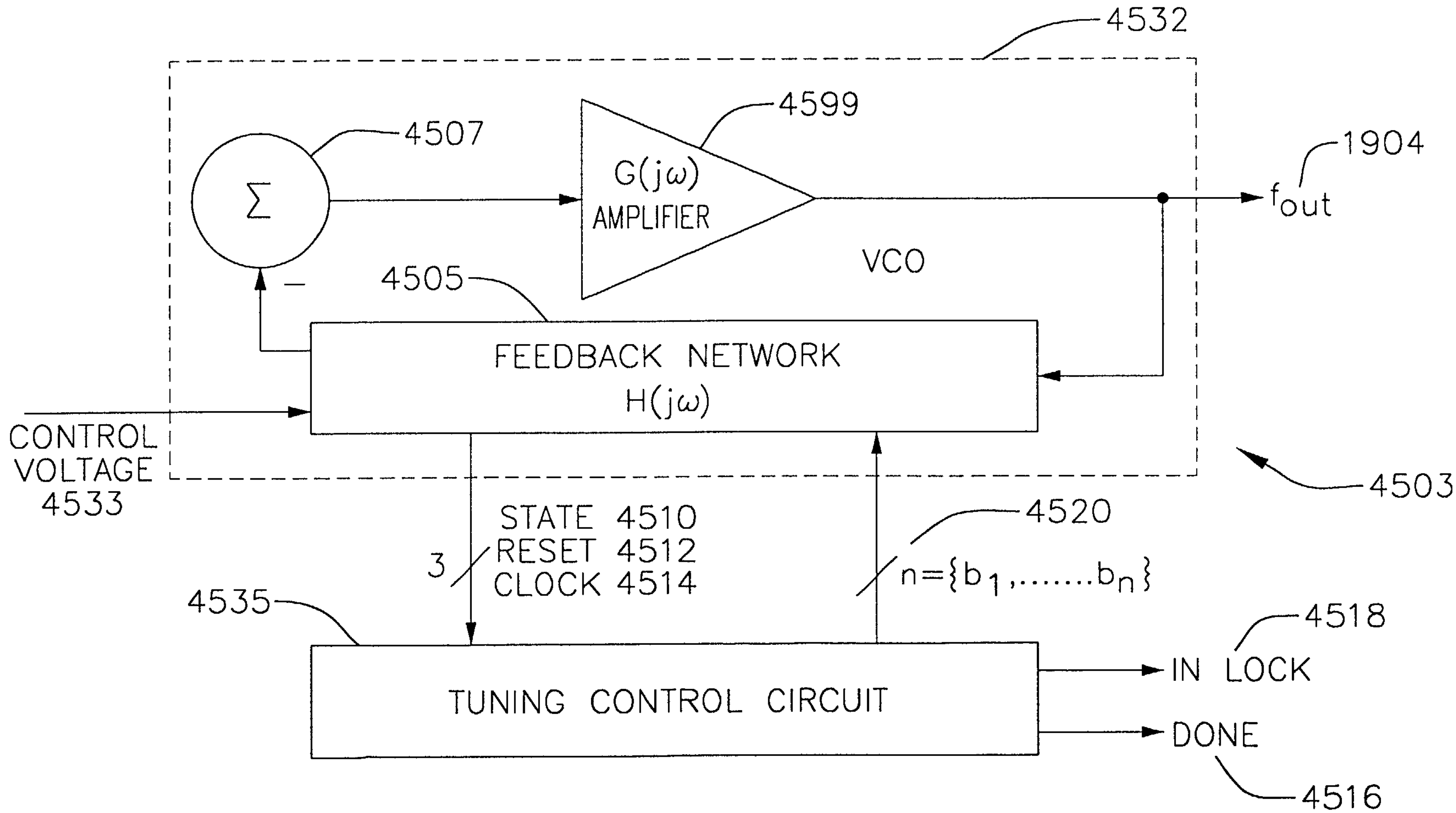

4503
4532
VCO
CONTROL
VOLTAGE
4533
f_{out}
1904
STATE 4510
RESET 4512
CLOCK 4514
3
4520
$n=\{b_1, \ldots\ldots b_n\}$
4535
TUNING CONTROL CIRCUIT
IN LOCK
4518
DONE
4516

FIG. 45d



4532
4507
Σ
4599
G(jω)
AMPLIFIER
1904
f out
VCO
4505
–
FEEDBACK NETWORK
H(jω)
CONTROL VOLTAGE 4533
4503
STATE 4510
RESET 4512
CLOCK 4514
3
4520
n={b 1,.......b n}
4535
4518
IN LOCK
TUNING CONTROL CIRCUIT
DONE
4516

FIG. 45e

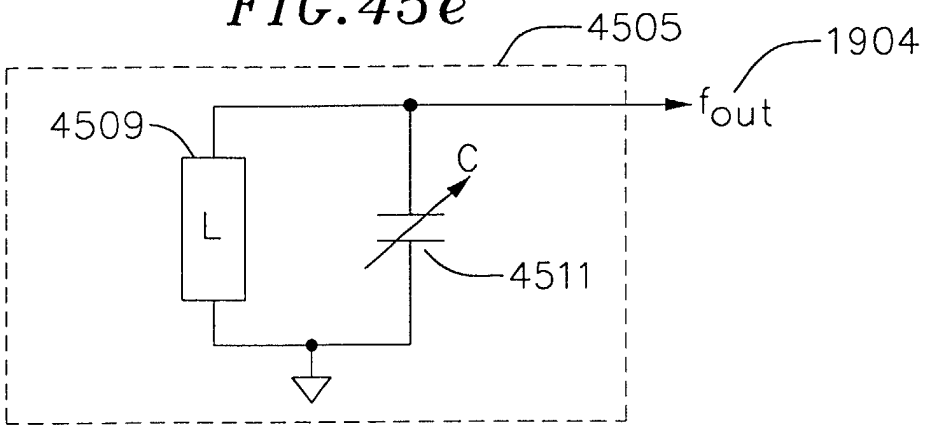


FIG. 45f

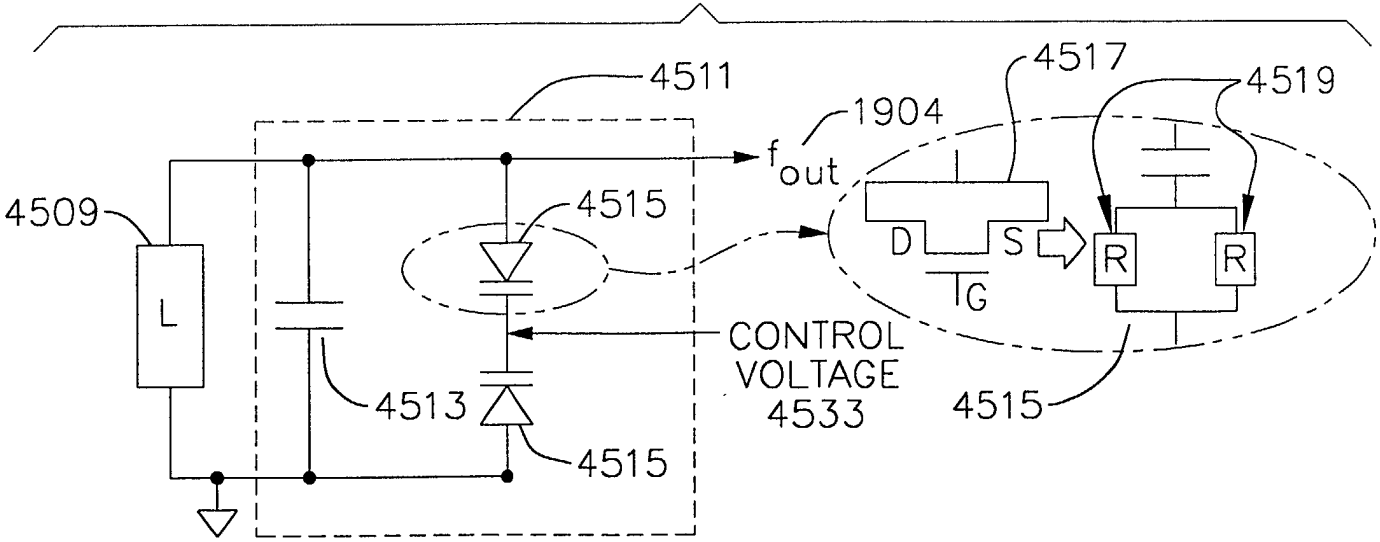


FIG. 45g

CAPACITANCE VS CONTROL VOLTAGE

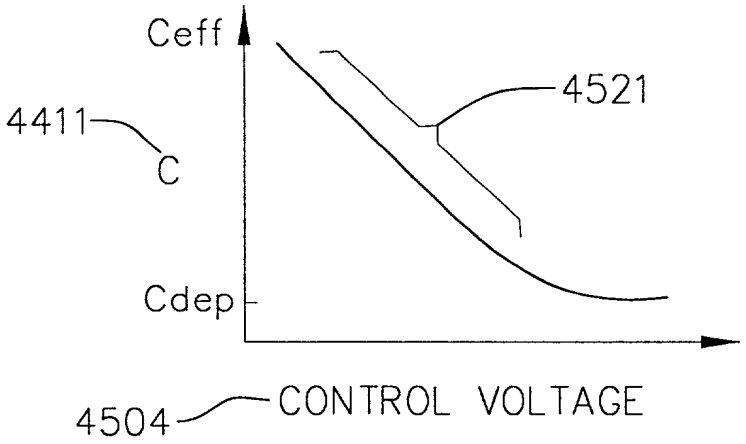


FIG. 45h

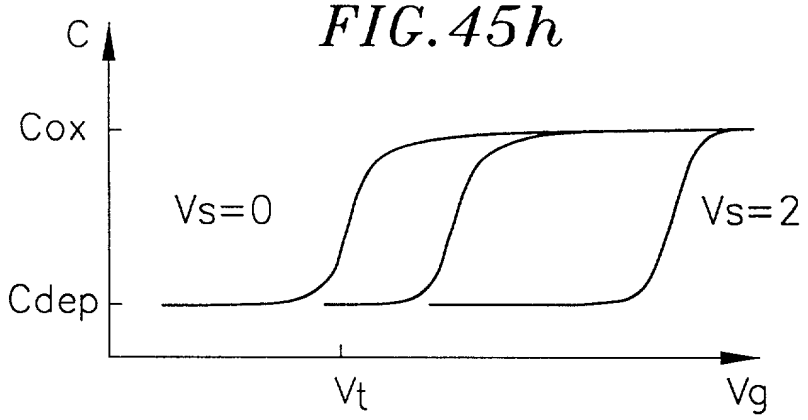


FIG. 45j

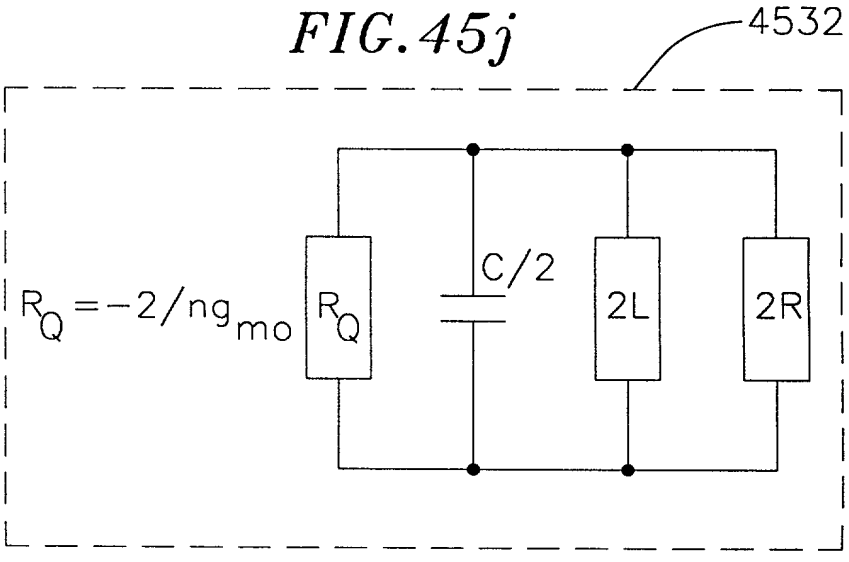


FIG. 45i

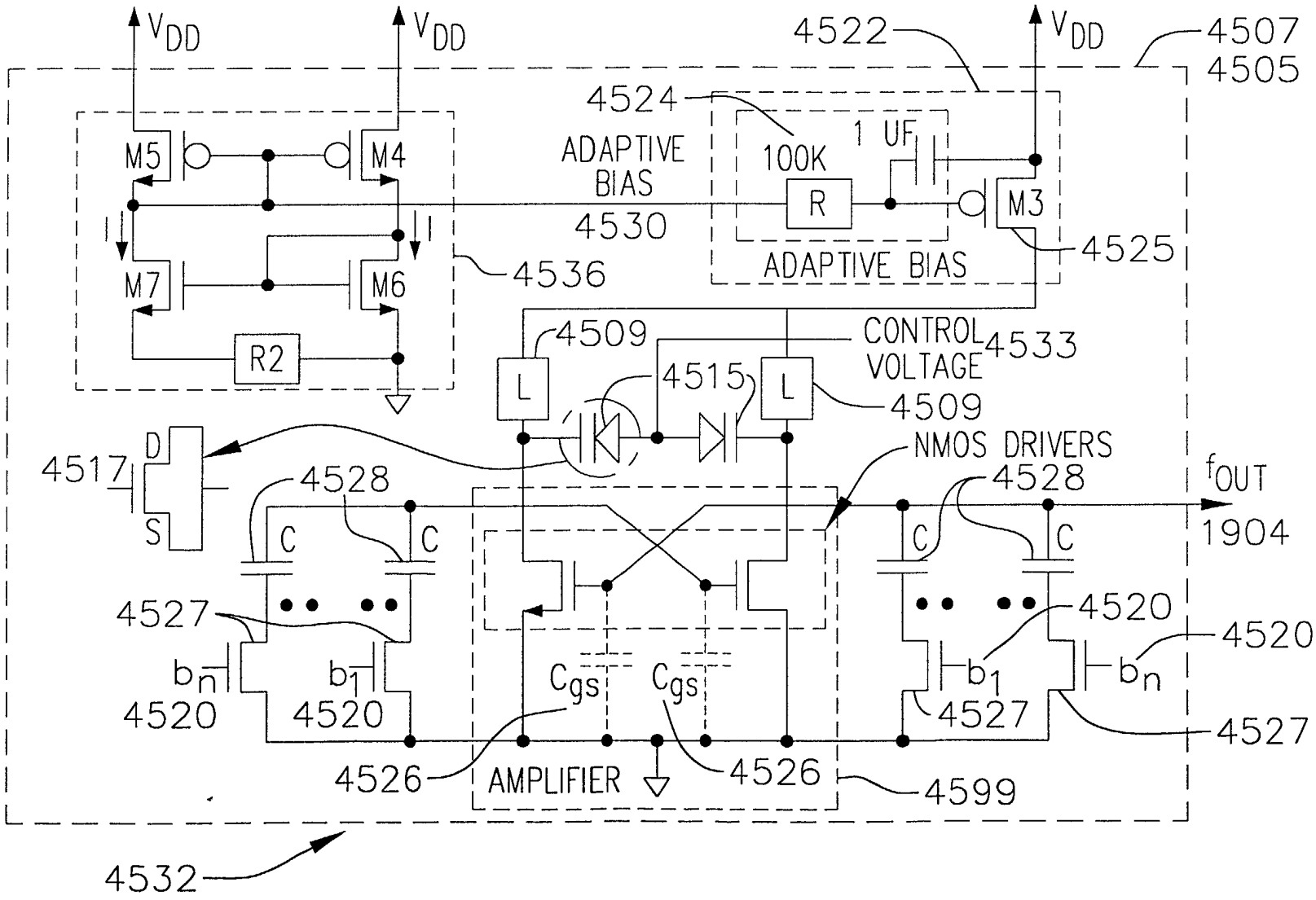

V_{DD}
V_{DD}
V_{DD}
4522
4507
4505
4524
100K
1 UF
ADAPTIVE BIAS
4530
M5
M4
M3
R
4525
ADAPTIVE BIAS
M7
M6
4536
R2
4509
CONTROL VOLTAGE
4533
L
4515
L
4509
4517
D
S
NMOS DRIVERS
4528
4528
f_{OUT}
1904
C
C
C
C
4527
4520
4520
b_n
b_1
C_{gs}
C_{gs}
b_1
b_n
4520
4527
4527
4526
AMPLIFIER
4526
4599
4532

FIG. 45k

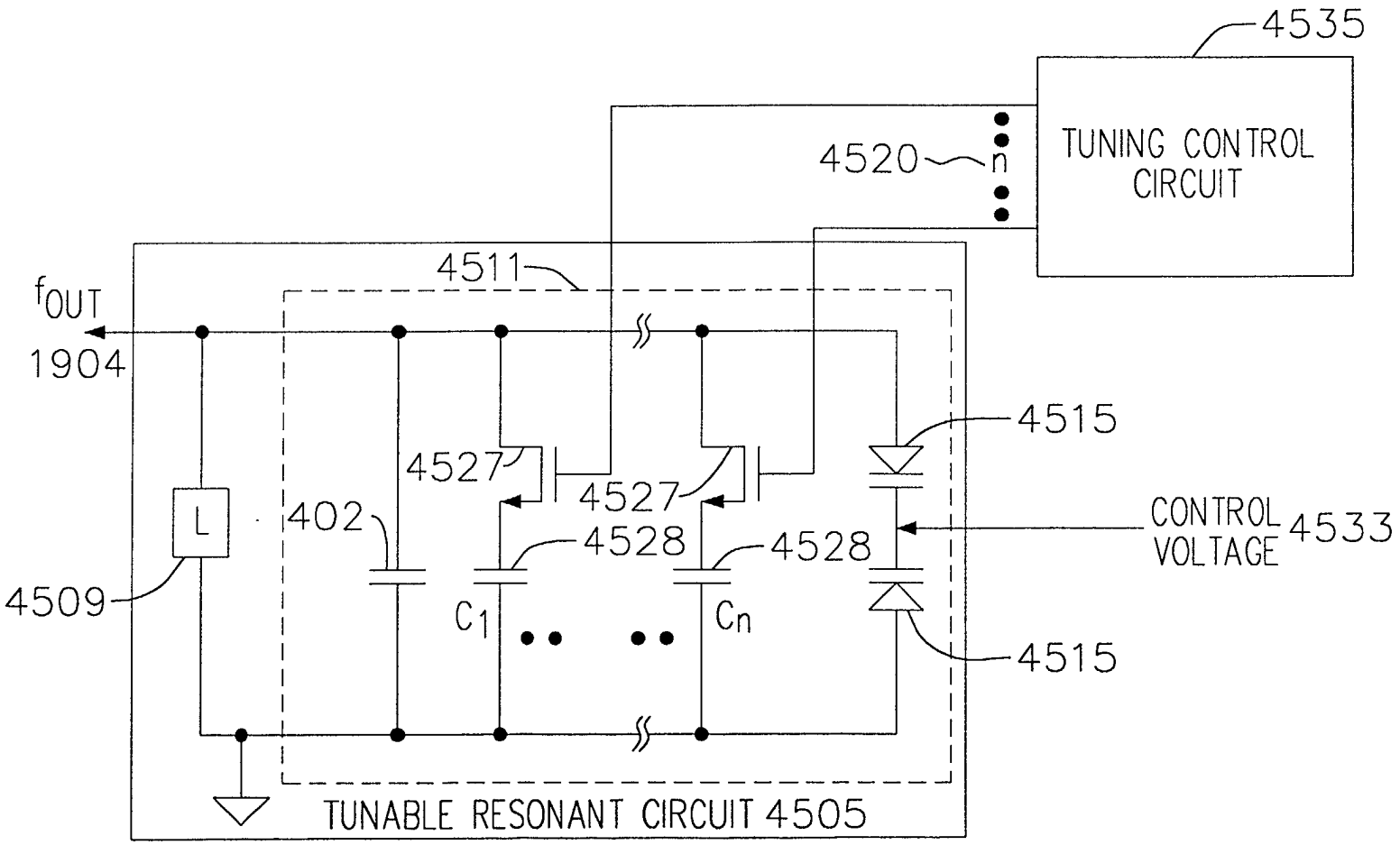
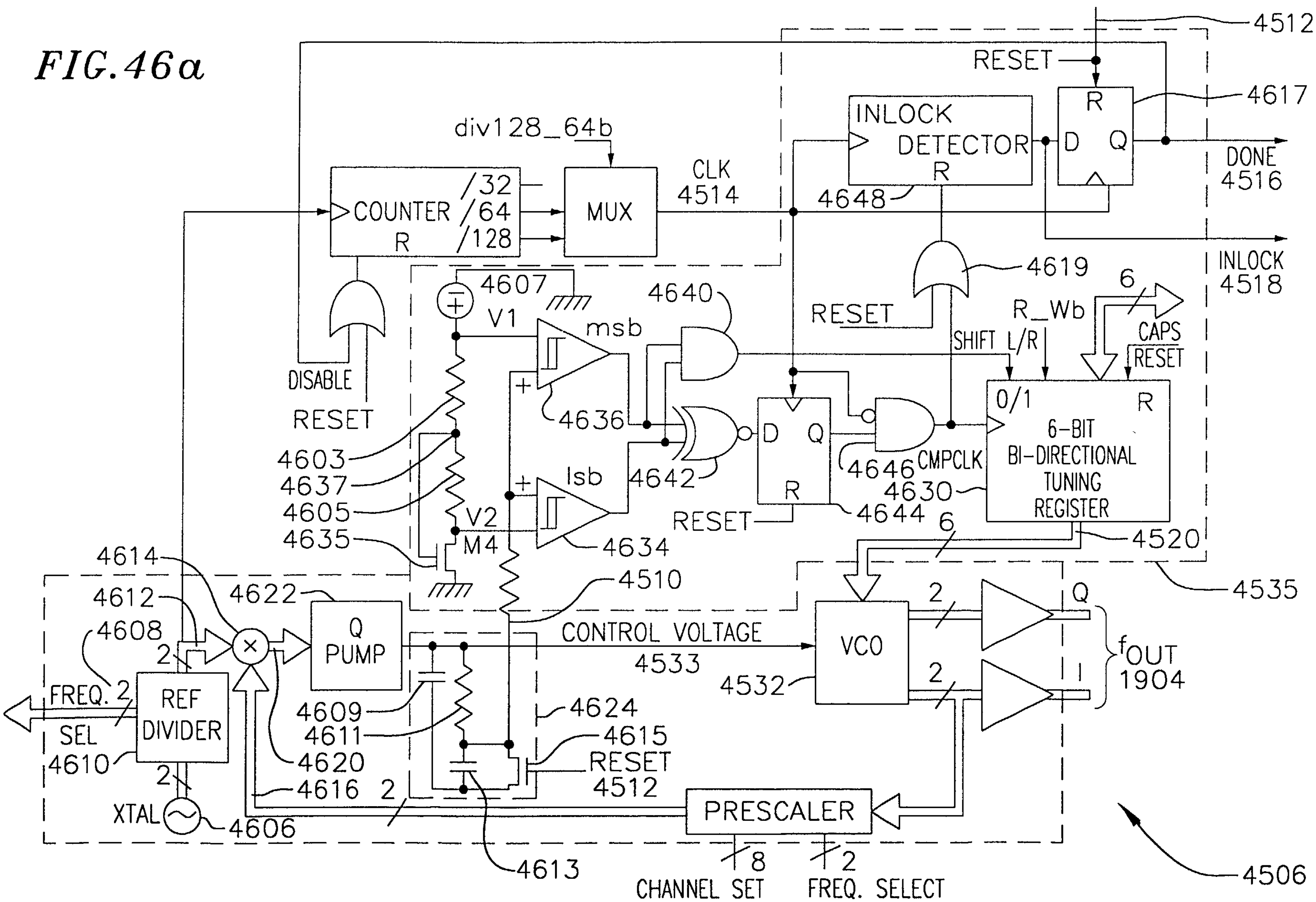


FIG. 46a



4512
RESET
R
D
Q
4617
INLOCK
DETECTOR
R
DONE
4516
INLOCK
4518
div128_64b
COUNTER
/32
/64
/128
R
MUX
CLK
4514
4648
4619
RESET
6
R_Wb
CAPS
RESET
SHIFT L/R
0/1
6-BIT
BI-DIRECTIONAL
TUNING
REGISTER
CMPCLK
4630
4646
4644
4520
4535
4607
V1
msb
lsb
4640
4642
4636
4634
DISABLE
RESET
4603
4637
4605
4635
V2
M4
4510
4614
4612
4608
4622
Q
PUMP
CONTROL VOLTAGE
4533
VCO
4532
2
fOUT
1904
FREQ. 2
SEL
4610
REF
DIVIDER
XTAL
4606
4609
4611
4620
4616
4624
4615
RESET
4512
4613
PRESCALER
8
CHANNEL SET
2
FREQ. SELECT
4506

FIG.46b

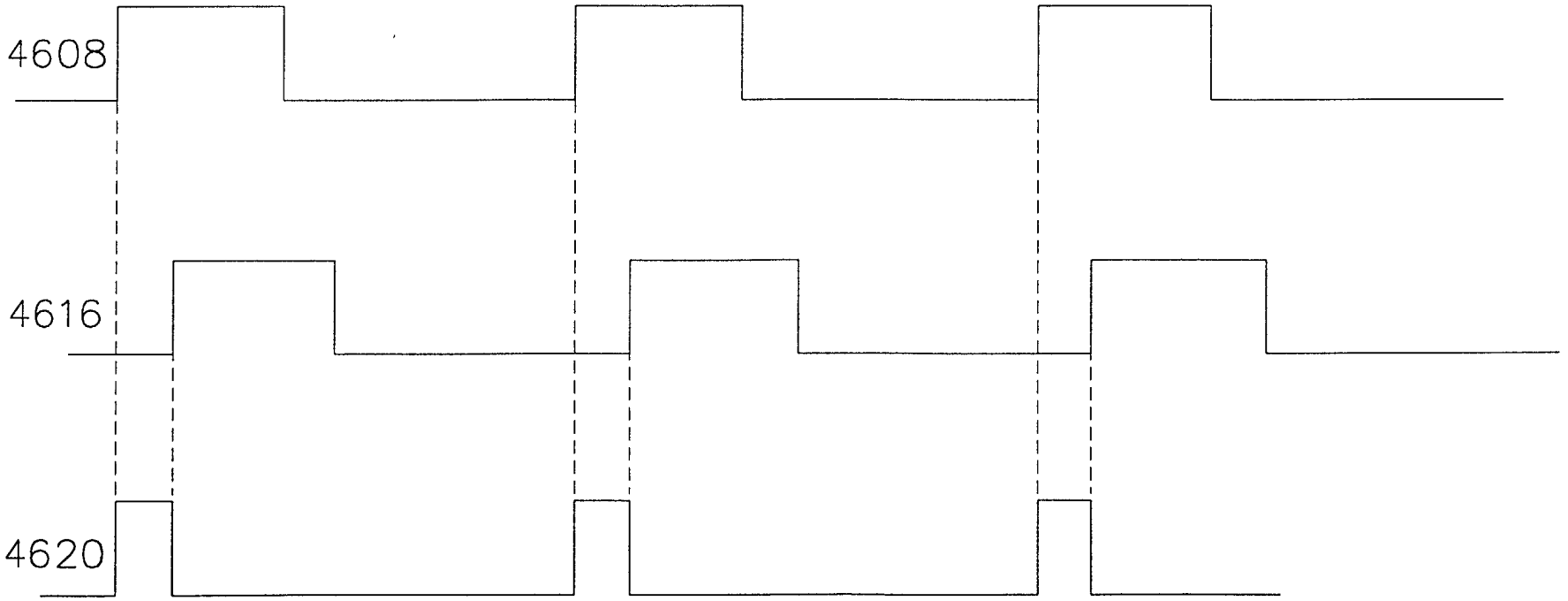


FIG. 47a

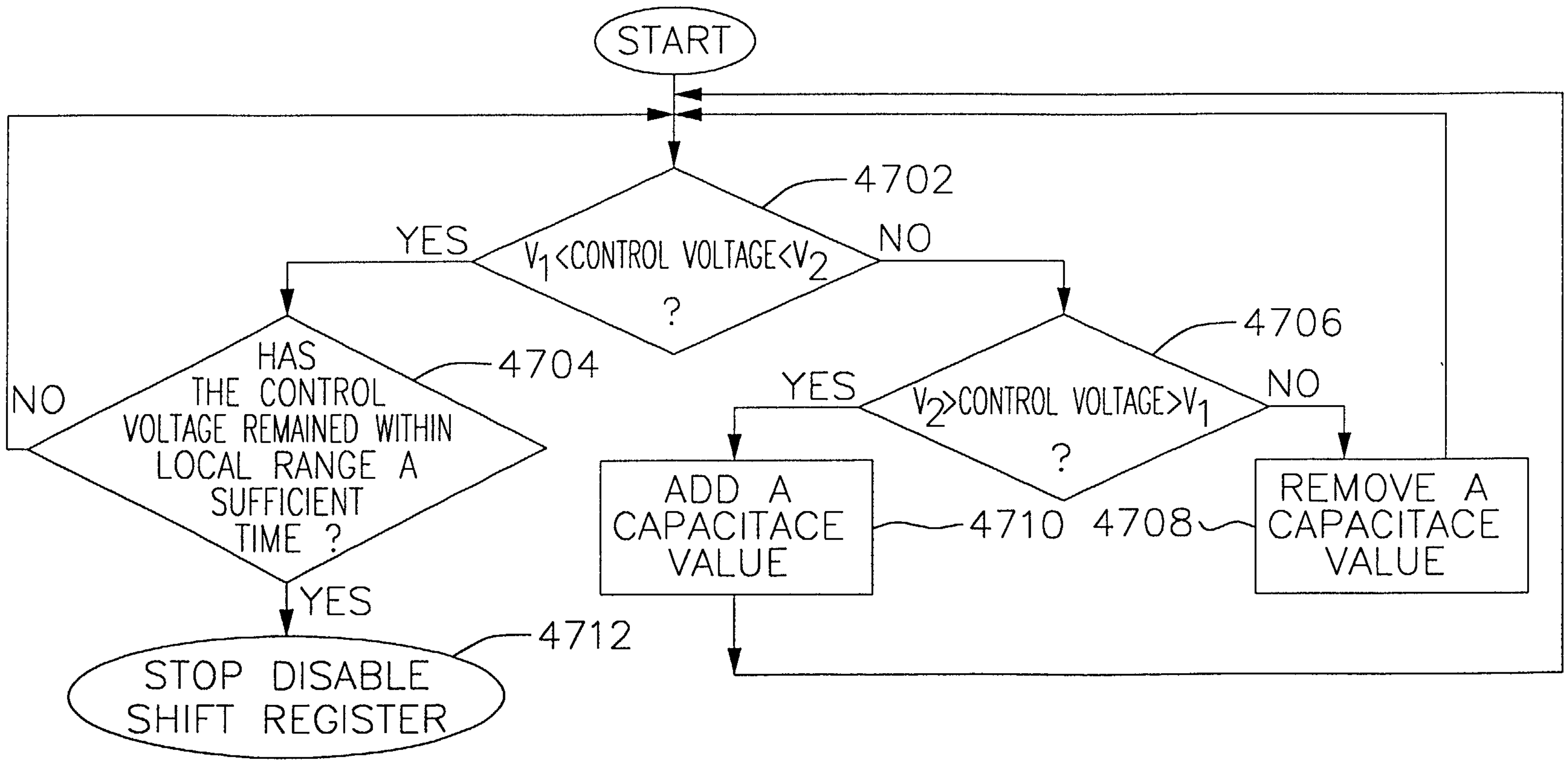
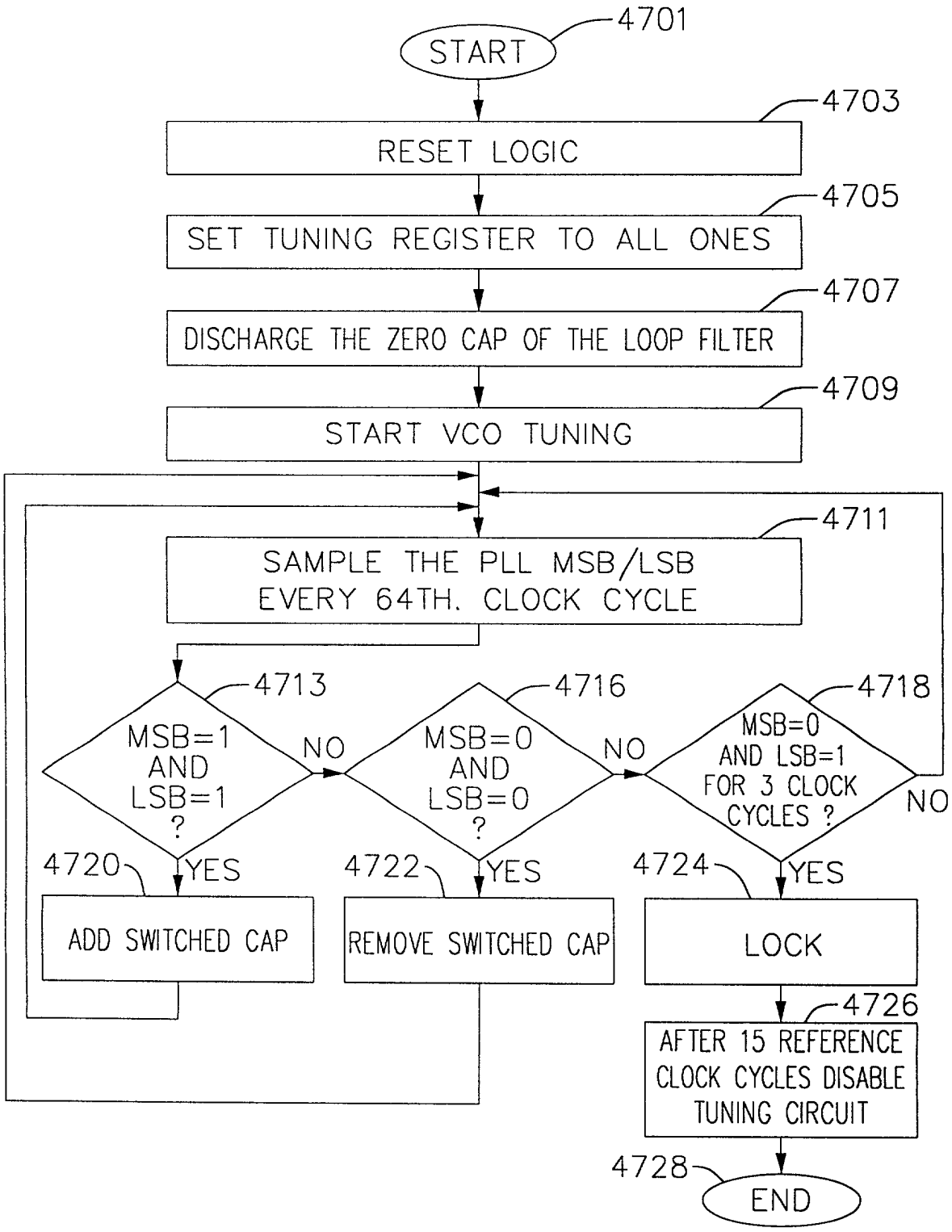

START
4702
V1<CONTROL VOLTAGE<V2 ?
YES
NO
HAS THE CONTROL VOLTAGE REMAINED WITHIN LOCAL RANGE A SUFFICIENT TIME ?
4704
NO
YES
STOP DISABLE SHIFT REGISTER
4712
4706
V2>CONTROL VOLTAGE>V1 ?
YES
NO
ADD A CAPACITACE VALUE
4710
4708
REMOVE A CAPACITACE VALUE

FIG. 47b


4701
START
4703
RESET LOGIC
4705
SET TUNING REGISTER TO ALL ONES
4707
DISCHARGE THE ZERO CAP OF THE LOOP FILTER
4709
START VCO TUNING
4711
SAMPLE THE PLL MSB/LSB EVERY 64TH. CLOCK CYCLE
4713
MSB=1 AND LSB=1 ?
NO
4716
MSB=0 AND LSB=0 ?
NO
4718
MSB=0 AND LSB=1 FOR 3 CLOCK CYCLES ?
NO
YES
4720
ADD SWITCHED CAP
YES
4722
REMOVE SWITCHED CAP
YES
4724
LOCK
4726
AFTER 15 REFERENCE CLOCK CYCLES DISABLE TUNING CIRCUIT
4728
END

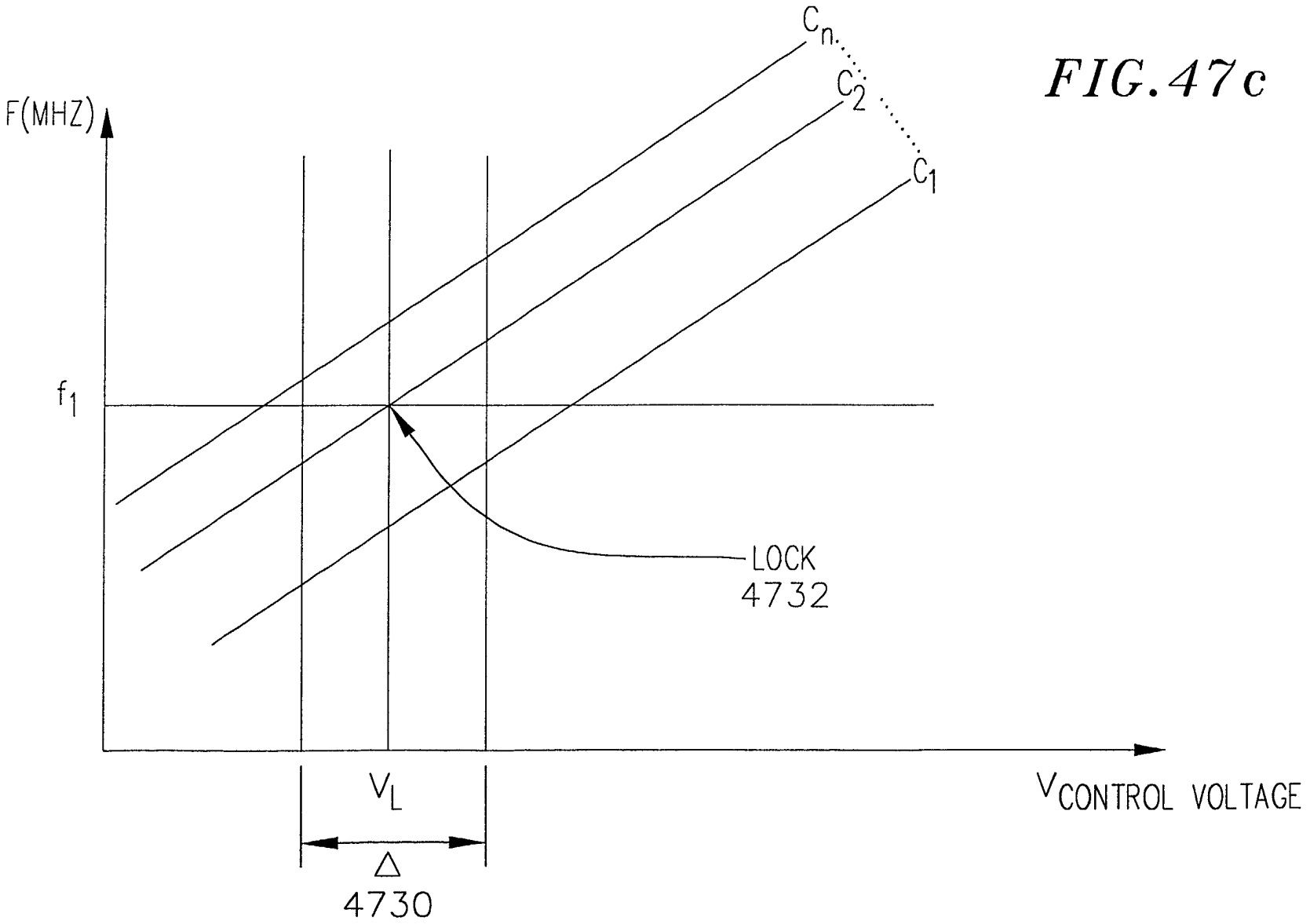


FIG.47c

FIG. 47d

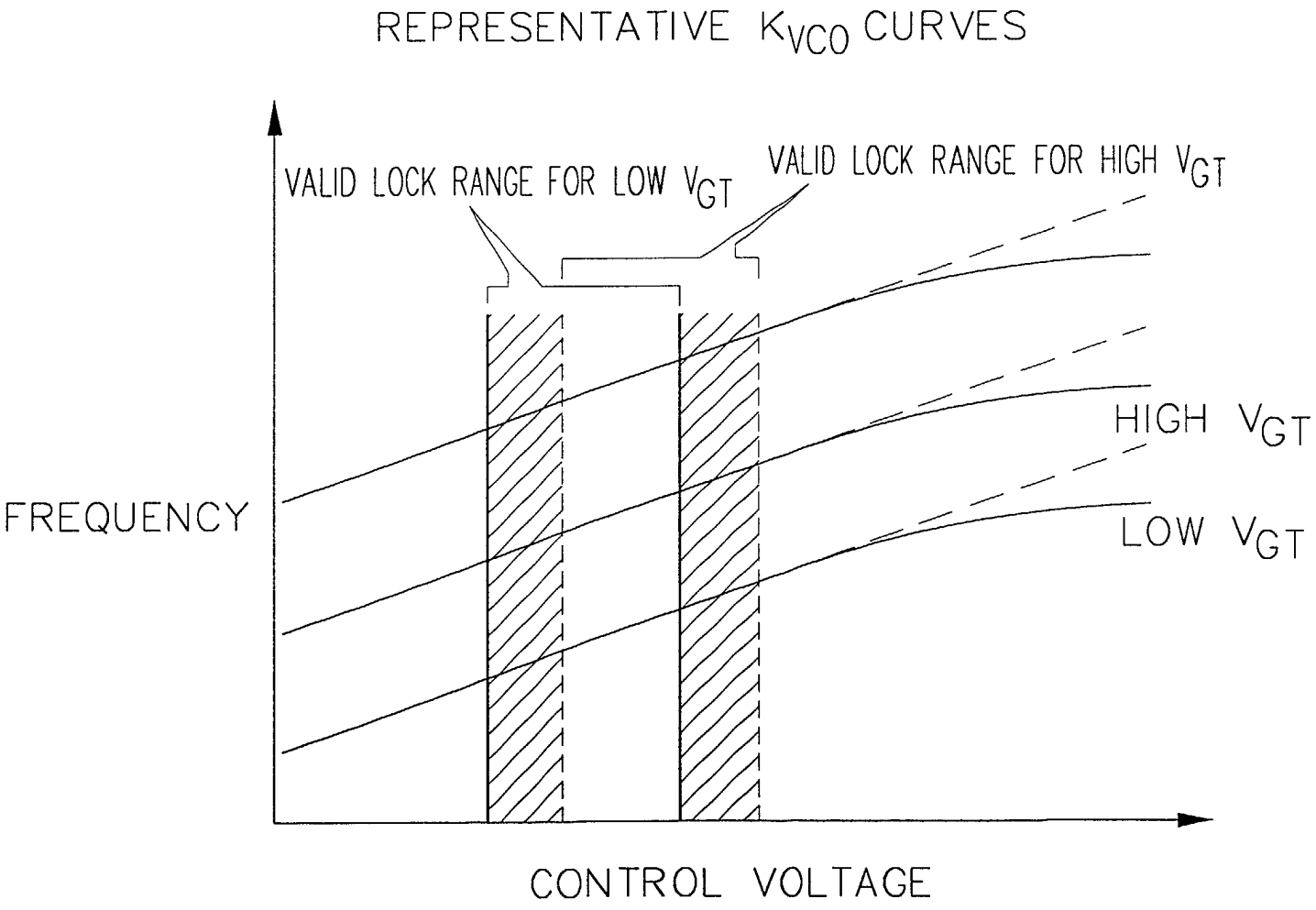

REPRESENTATIVE K_{VCO} CURVES
VALID LOCK RANGE FOR LOW V_{GT}
VALID LOCK RANGE FOR HIGH V_{GT}
HIGH V_{GT}
LOW V_{GT}
FREQUENCY
CONTROL VOLTAGE

FIG. 48

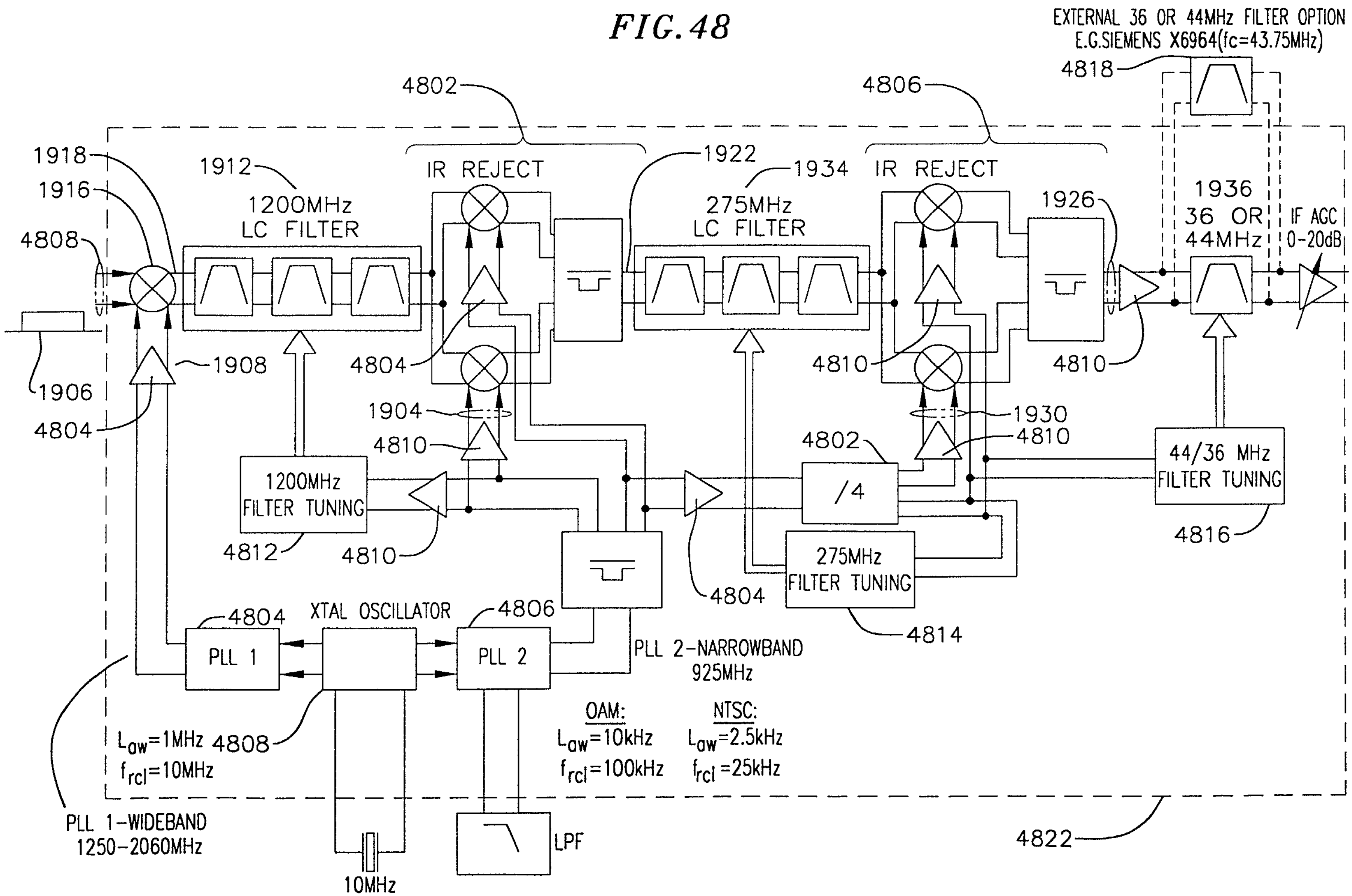
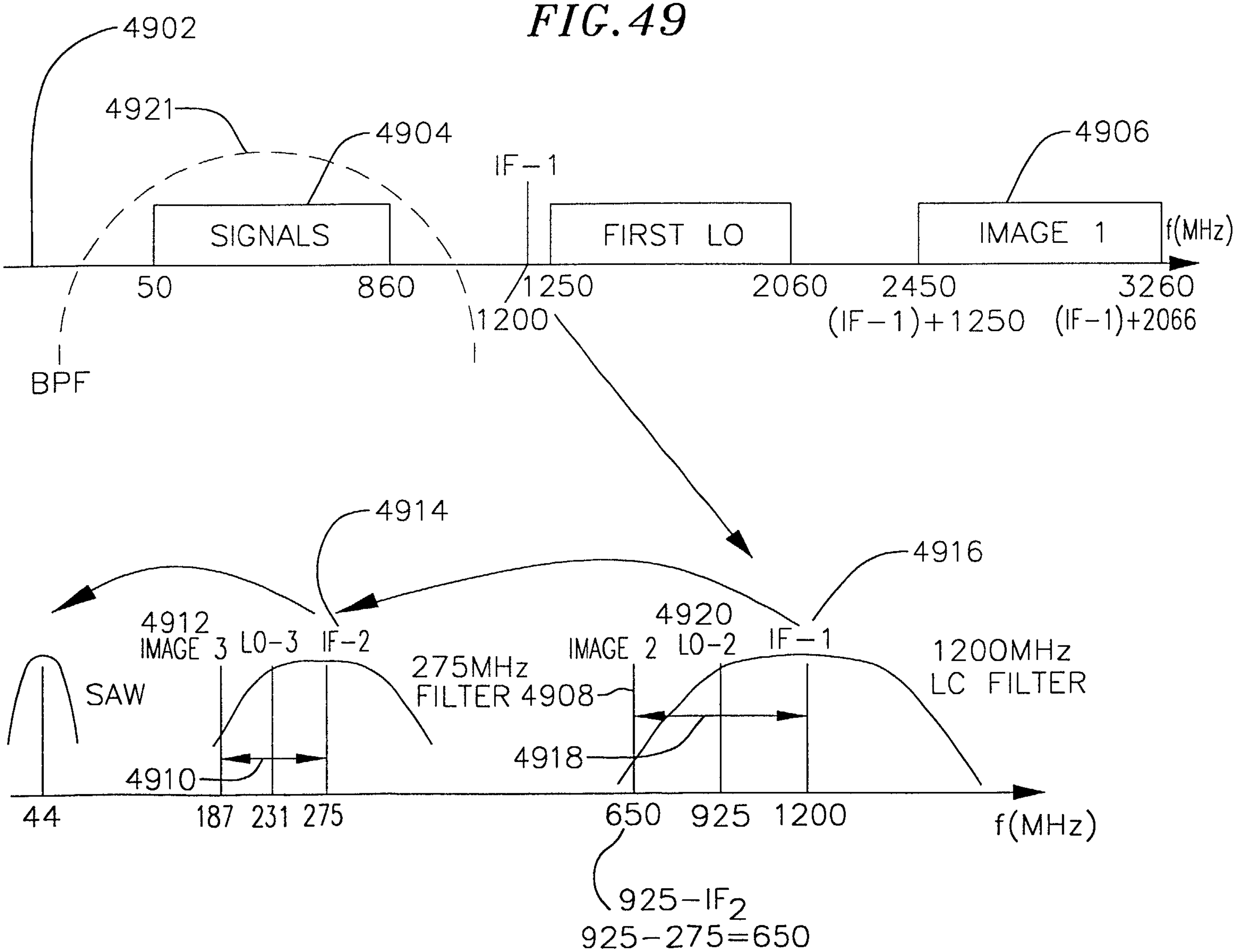

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
4818
4802
4806
1918
1916
4808
1906
4804
1908
1912
1200MHz
LC FILTER
IR REJECT
4804
1904
4810
1200MHz
FILTER TUNING
4812
4810
1922
1934
275MHz
LC FILTER
IR REJECT
4810
1930
4810
4802
/4
275MHz
FILTER TUNING
4814
4804
1926
4810
1936
36 OR
44MHz
IF AGC
0-20dB
44/36 MHz
FILTER TUNING
4816
4804
XTAL OSCILLATOR
4806
PLL 1
PLL 2
PLL 2-NARROWBAND
925MHz
L_{aw}=1MHz
f_{rcl}=10MHz
4808
OAM:
L_{aw}=10kHz
f_{rcl}=100kHz
NTSC:
L_{aw}=2.5kHz
f_{rcl}=25kHz
PLL 1-WIDEBAND
1250-2060MHz
10MHz
LPF
4822

FIG. 49



4902
4921
4904
IF-1
4906
SIGNALS
FIRST LO
IMAGE 1
f(MHz)
50
860
1250
1200
2060
2450
3260
(IF-1)+1250
(IF-1)+2066
BPF
4914
4916
4912
IMAGE 3
LO-3
IF-2
4920
IMAGE 2
LO-2
IF-1
275MHz
FILTER 4908
1200MHz
LC FILTER
SAW
4910
4918
44
187
231
275
650
925
1200
f(MHz)
925-IF2
925-275=650

FIG. 50

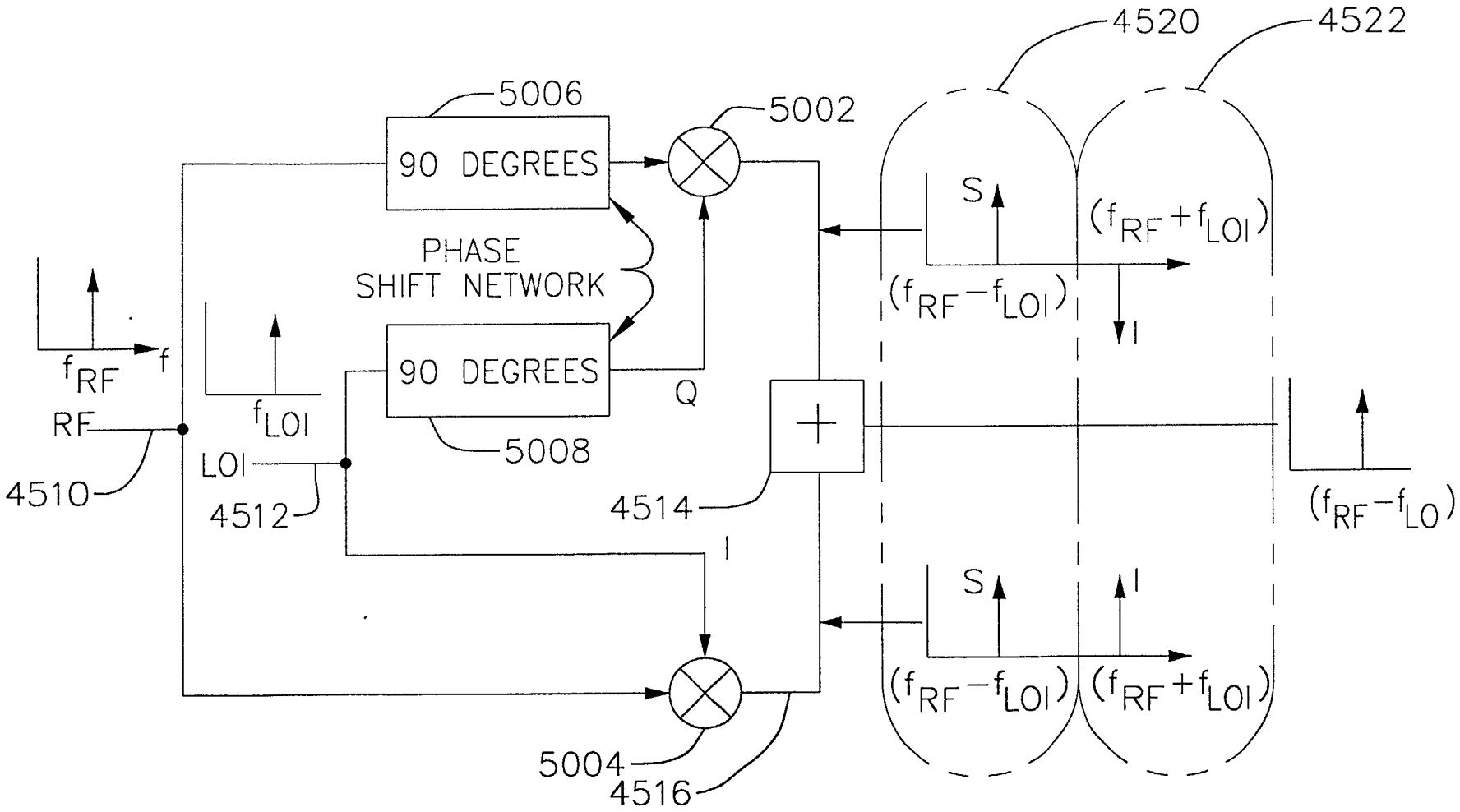

4520
4522
5006
5002
90 DEGREES
PHASE
SHIFT NETWORK
90 DEGREES
5008
Q
I
S
I
$(f_{RF}+f_{LOI})$
$(f_{RF}-f_{LOI})$
f_{RF}
f
RF
4510
f_{LOI}
LOI
4512
4514
$(f_{RF}-f_{LO})$
S
I
$(f_{RF}-f_{LOI})$
$(f_{RF}+f_{LOI})$
5004
4516

FIG.51

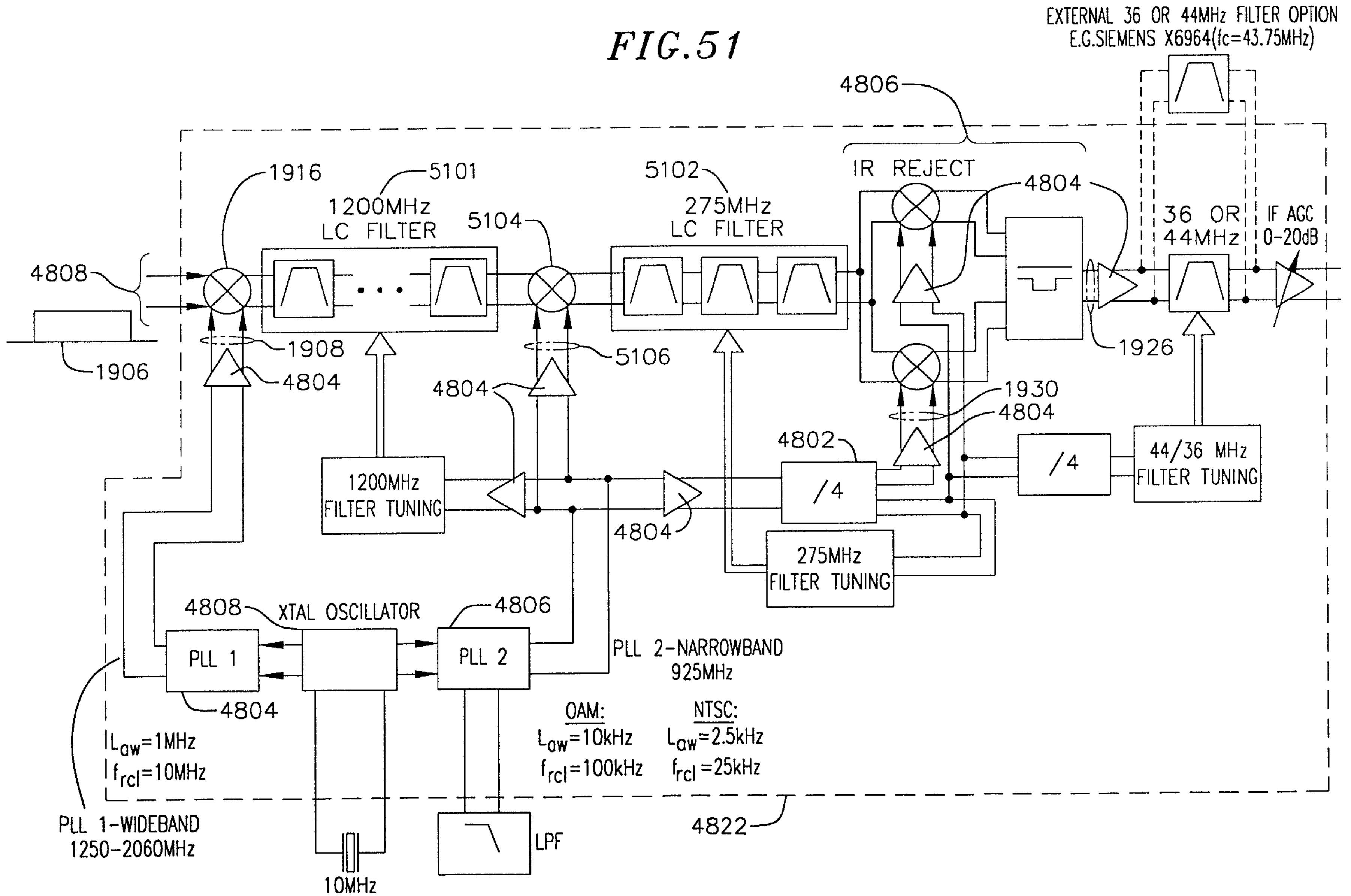

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
4806
IR REJECT
4804
36 OR 44MHz
IF AGC 0-20dB
1916
5101
1200MHz LC FILTER
5104
5102
275MHz LC FILTER
4808
1908
1906
4804
5106
1926
1930
4802
/4
44/36 MHz FILTER TUNING
1200MHz FILTER TUNING
275MHz FILTER TUNING
4808
XTAL OSCILLATOR
4806
PLL 1
PLL 2
PLL 2-NARROWBAND 925MHz
OAM:
L_{aw}=10kHz
f_{rcl}=100kHz
NTSC:
L_{aw}=2.5kHz
f_{rcl}=25kHz
L_{aw}=1MHz
f_{rcl}=10MHz
PLL 1-WIDEBAND 1250-2060MHz
10MHz
LPF
4822

FIG. 52

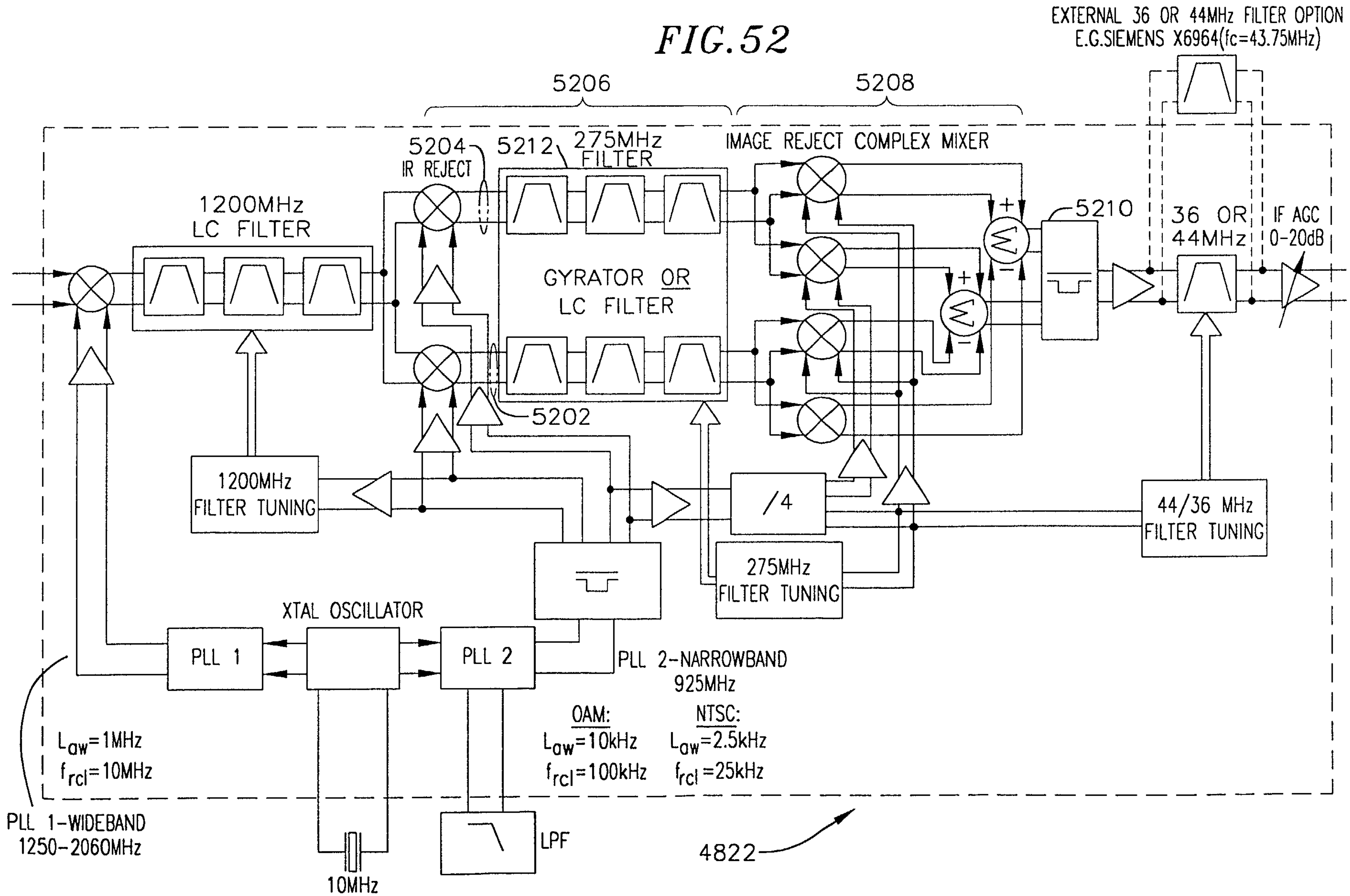

EXTERNAL 36 OR 44MHz FILTER OPTION
E.G.SIEMENS X6964(fc=43.75MHz)
5206
5208
5204
IR REJECT
5212
275MHz
FILTER
IMAGE REJECT COMPLEX MIXER
1200MHz
LC FILTER
GYRATOR OR
LC FILTER
5210
36 OR
44MHz
IF AGC
0-20dB
5202
1200MHz
FILTER TUNING
/4
44/36 MHz
FILTER TUNING
275MHz
FILTER TUNING
XTAL OSCILLATOR
PLL 1
PLL 2
PLL 2-NARROWBAND
925MHz
OAM:
L_{aw}=10kHz
f_{rcl}=100kHz
NTSC:
L_{aw}=2.5kHz
f_{rcl}=25kHz
L_{aw}=1MHz
f_{rcl}=10MHz
PLL 1-WIDEBAND
1250-2060MHz
10MHz
LPF
4822

FIG.53

CATV TUNER

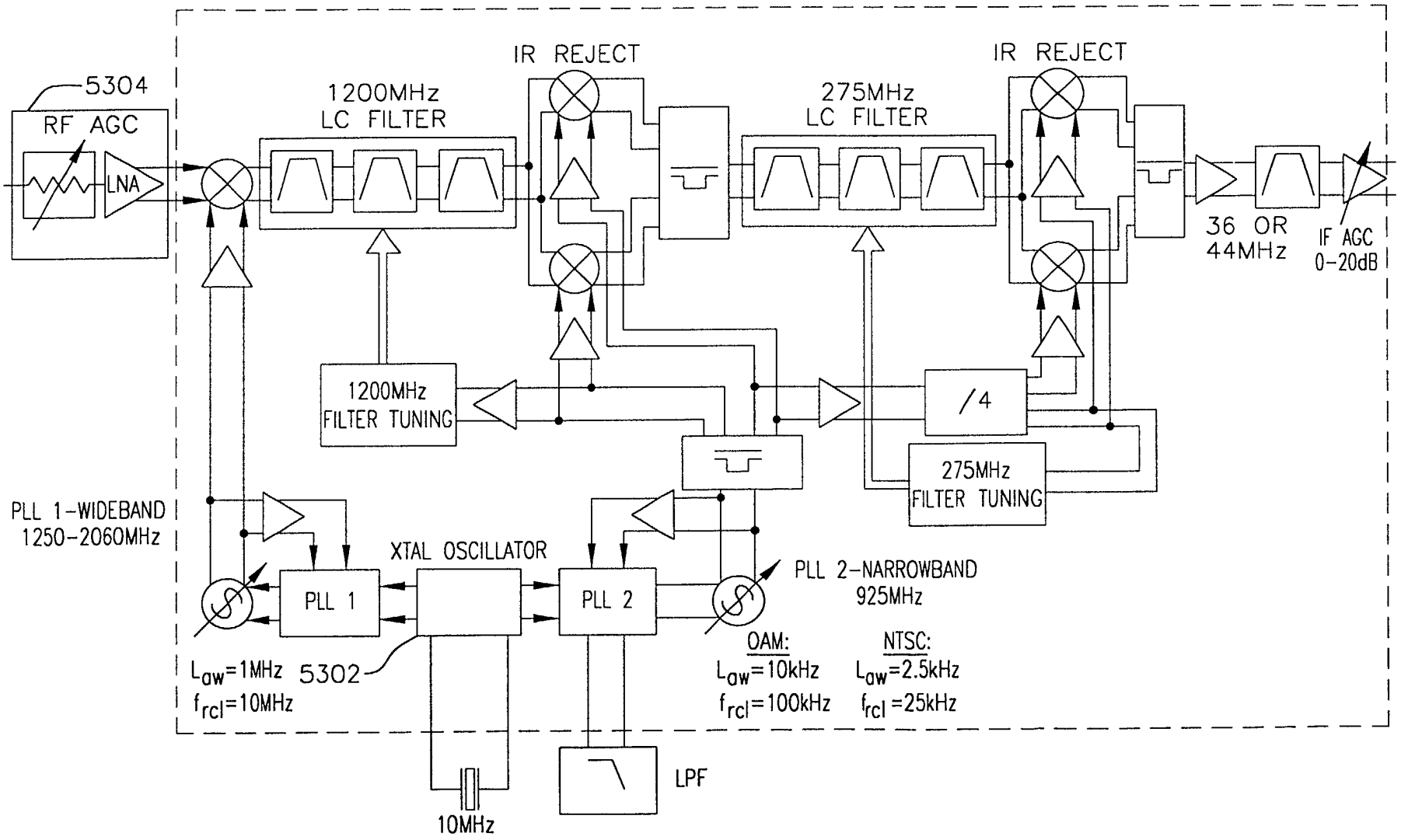


FIG.54

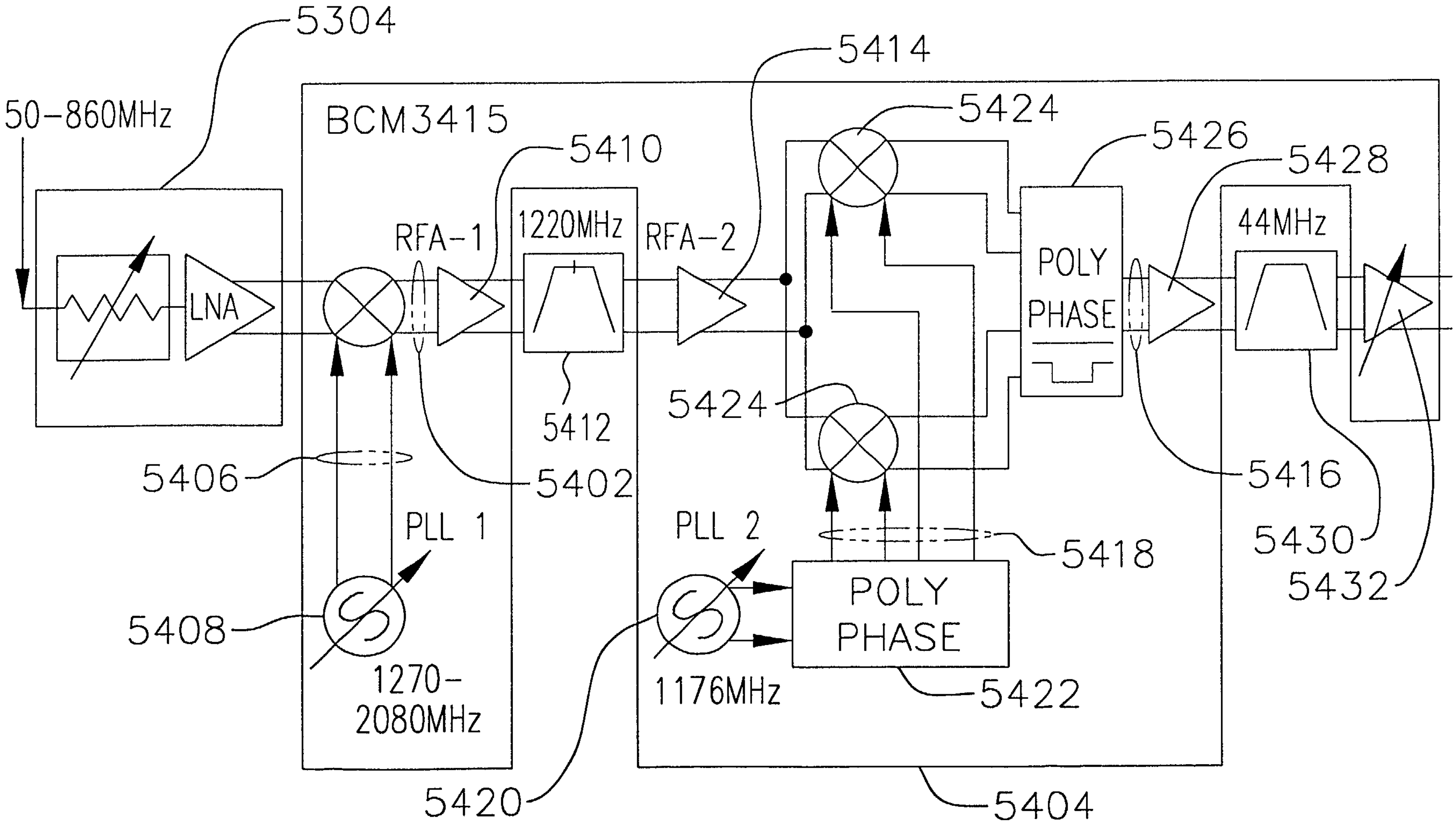

5304
50-860MHz
LNA
BCM3415
RFA-1
5410
1220MHz
5412
RFA-2
5414
5424
5424
5426
POLY
PHASE
5428
44MHz
5406
5402
5408
PLL 1
1270-
2080MHz
PLL 2
1176MHz
POLY
PHASE
5418
5422
5420
5404
5416
5430
5432

FIG.55

SET-TOP BOX

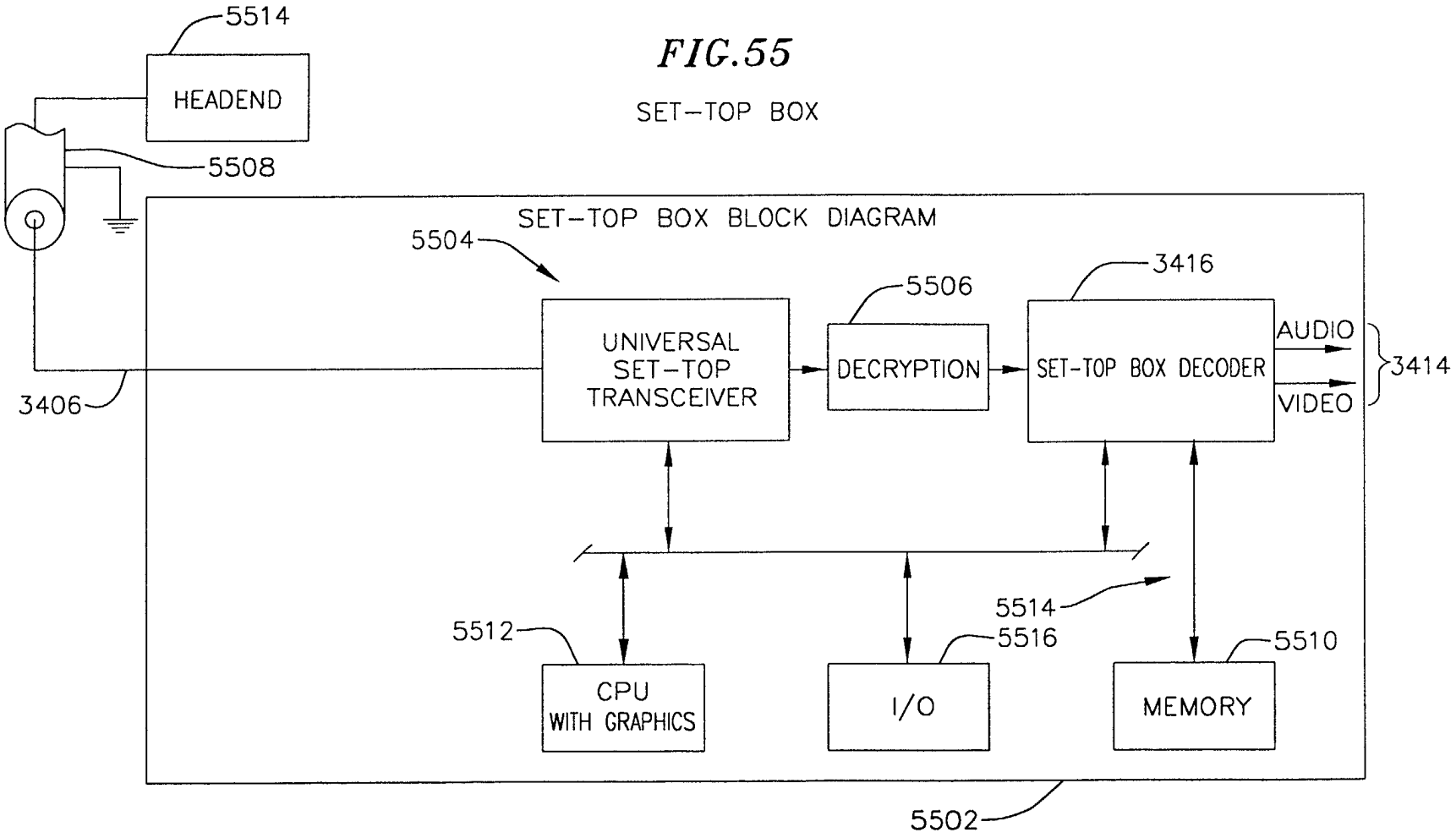


FIG.56

TELEVISION

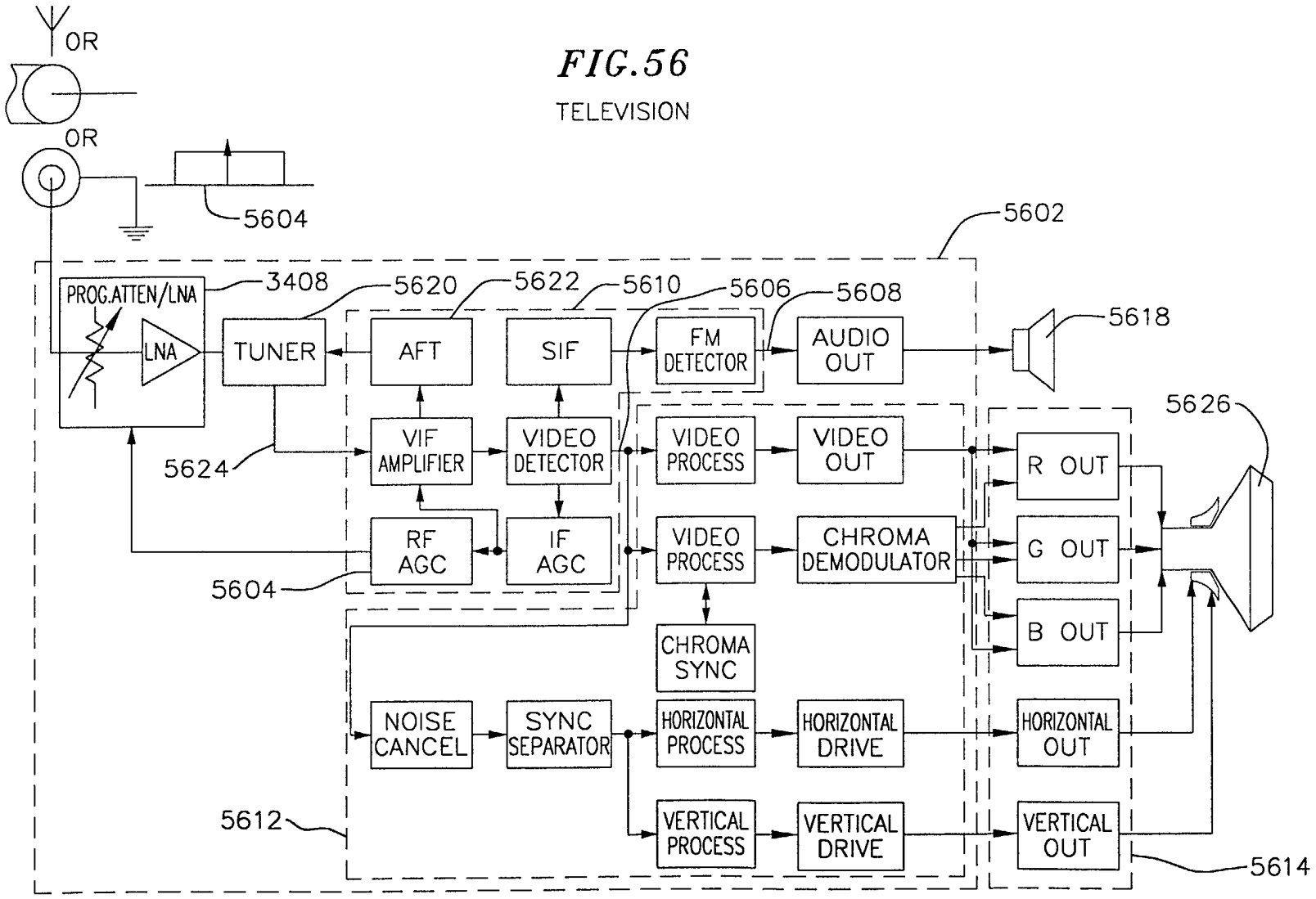


FIG.57

VCR BLOCK DIAGRAM

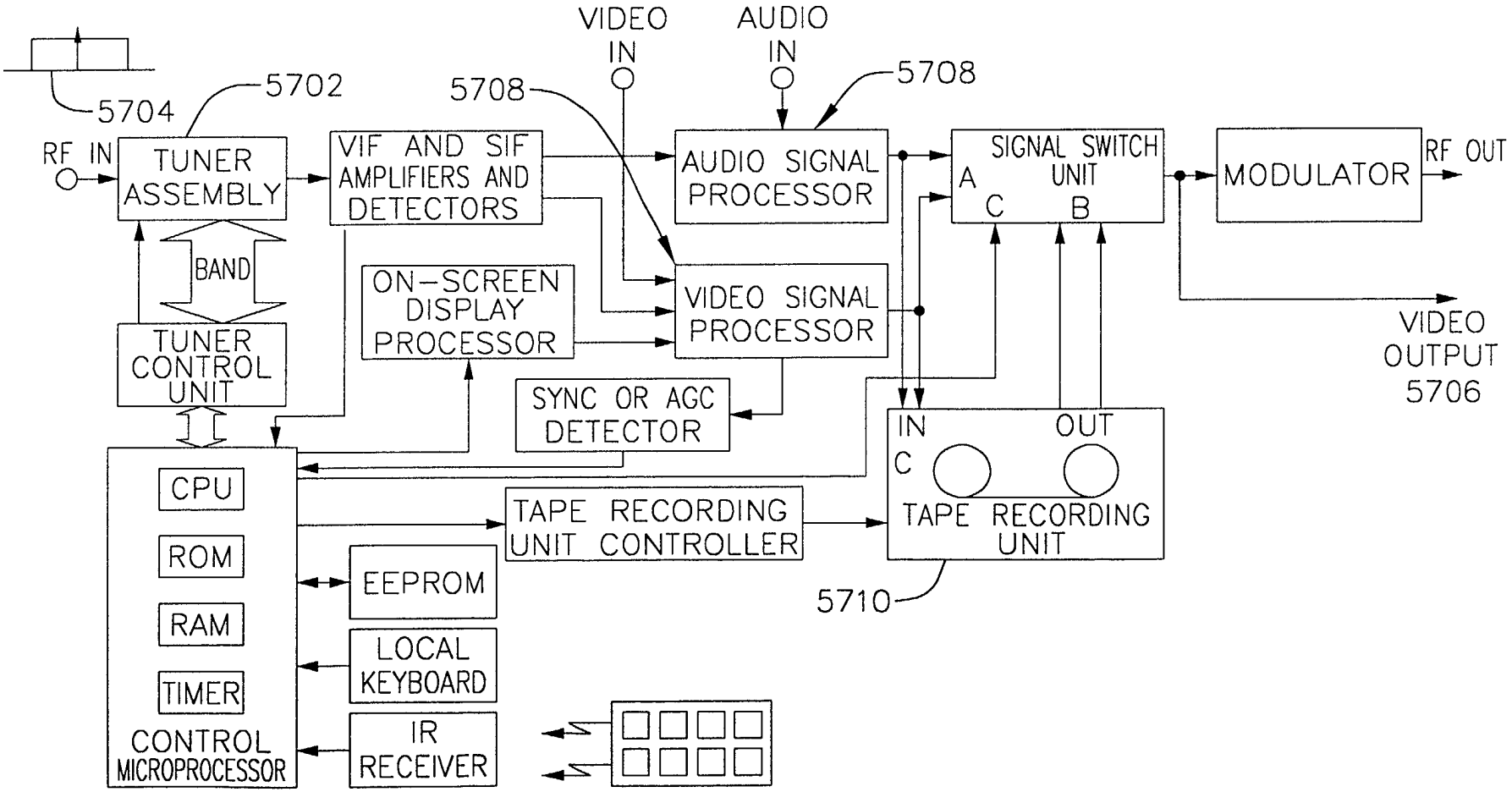


FIG.58

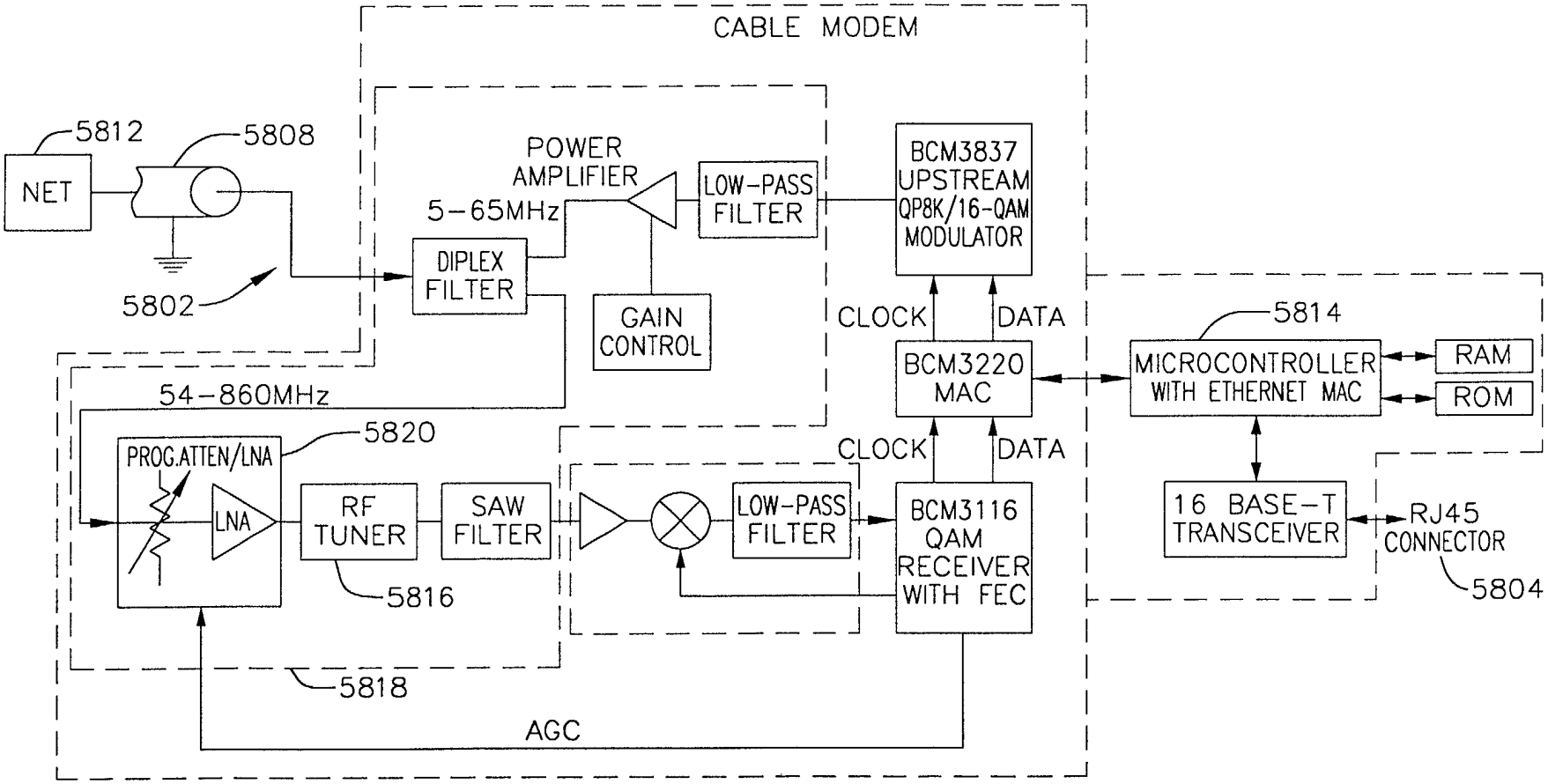


FIG.59

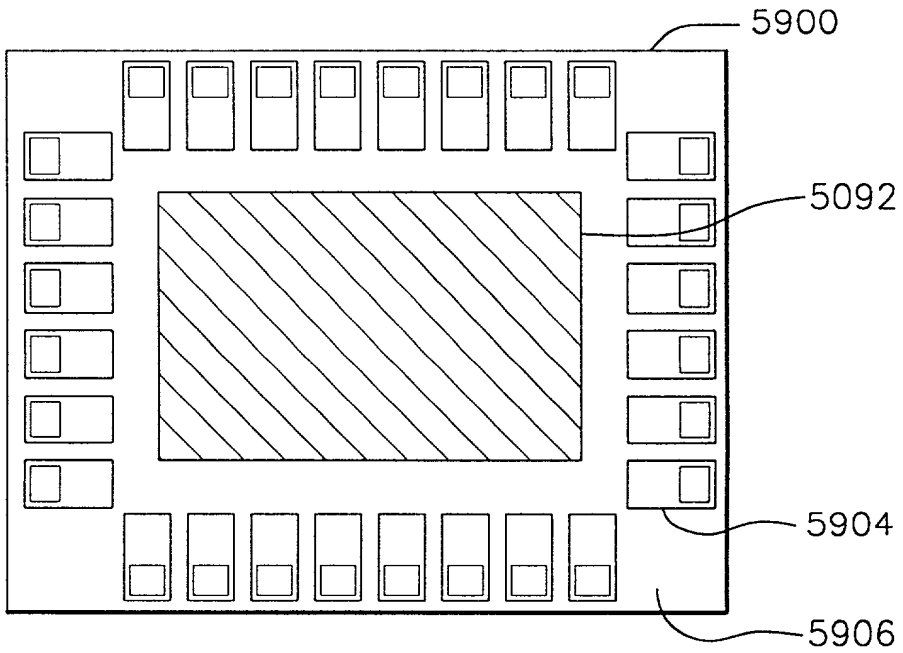


FIG.60

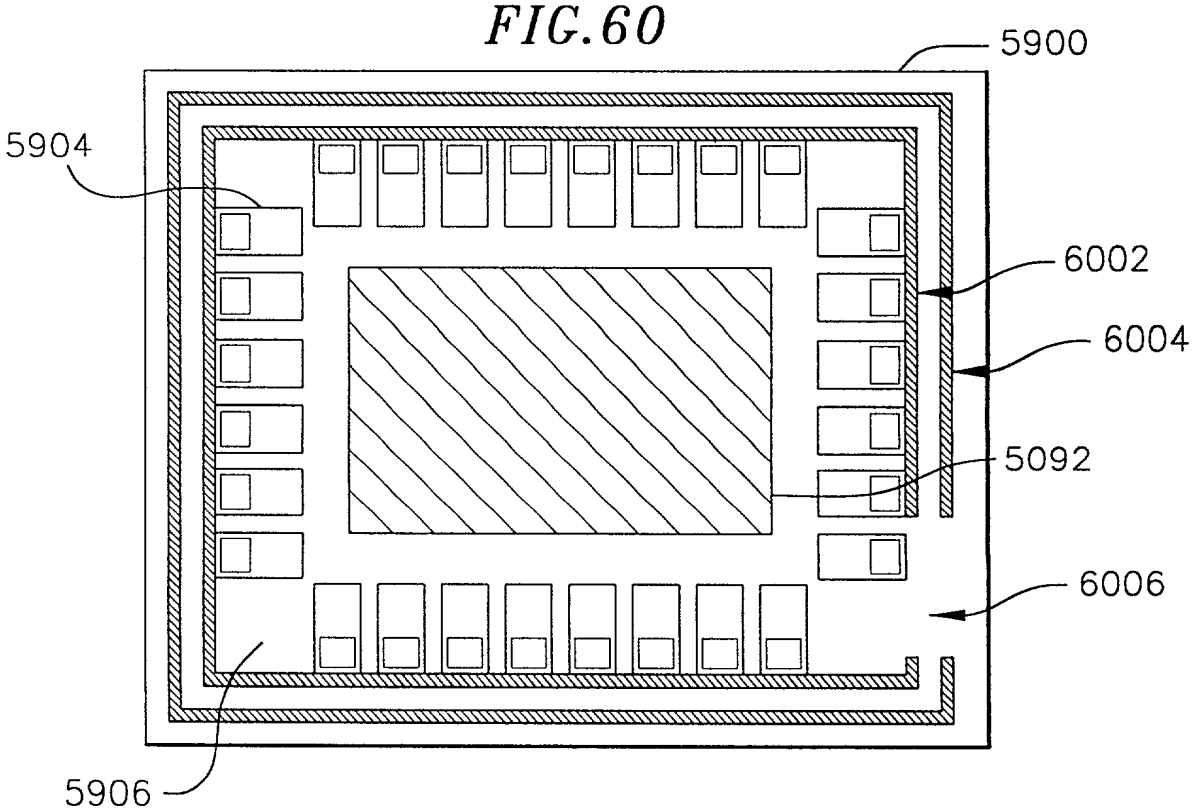


FIG.61

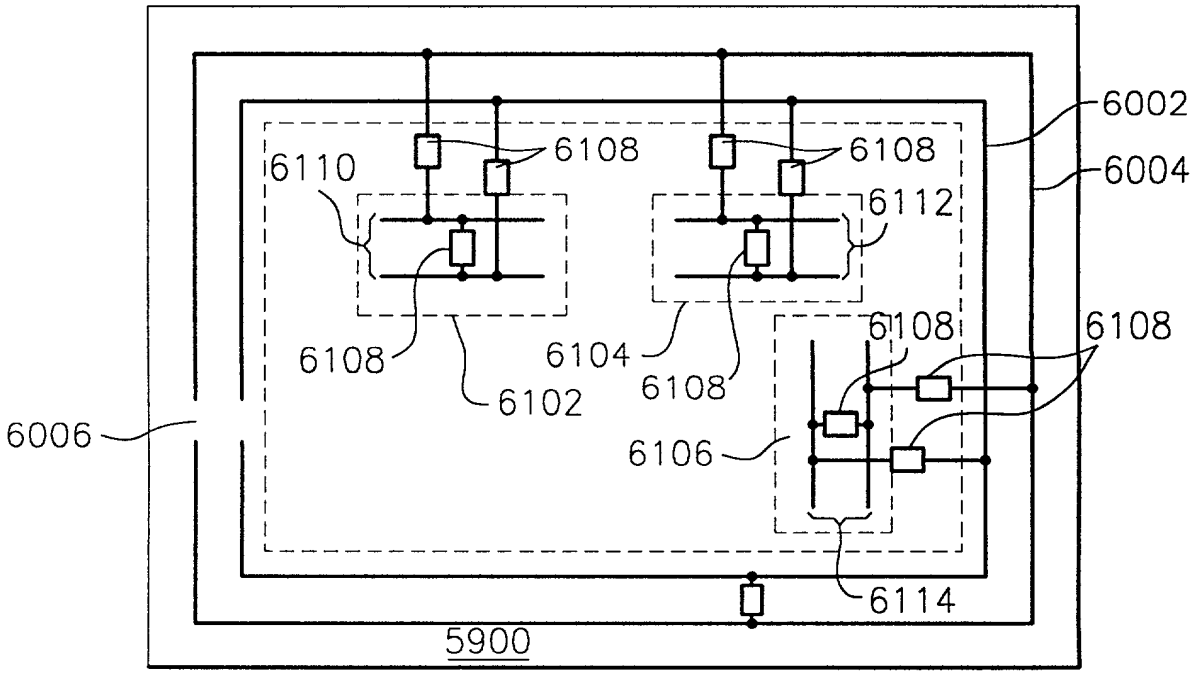

6002
6004
6110
6108
6108
6112
6108
6108
6104
6108
6102
6006
6106
6114
5900

FIG.62

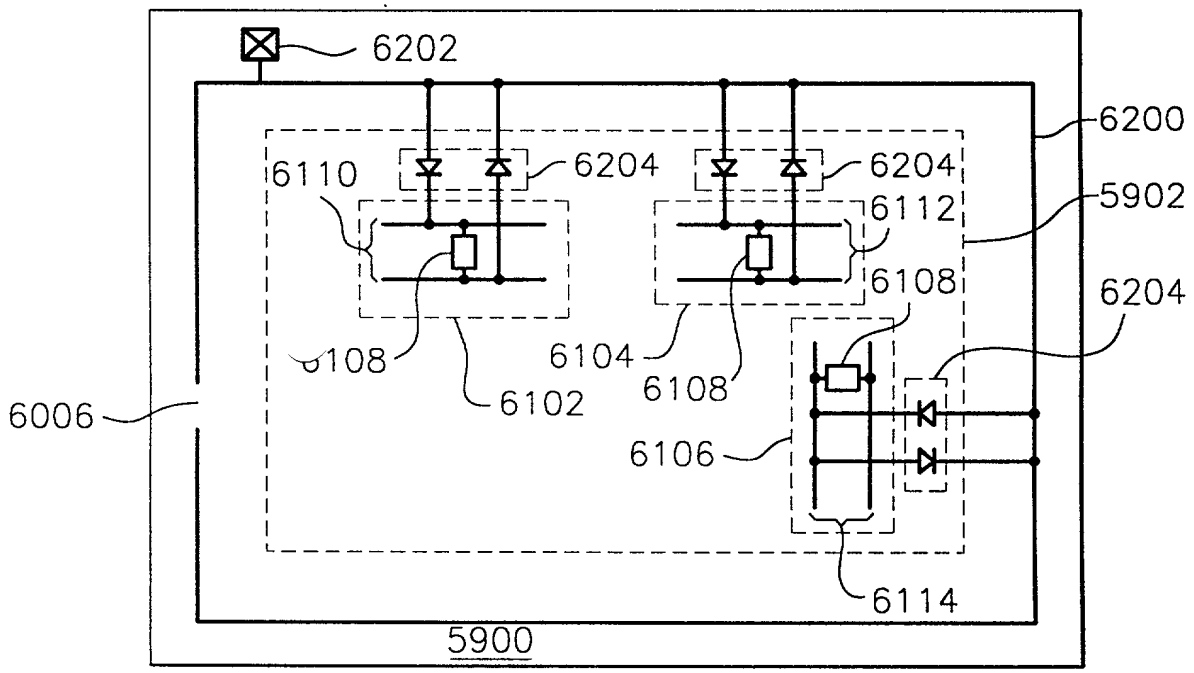

6202
6200
6110
6204
6204
6112
5902
6108
6204
6108
6104
6108
6102
6006
6106
6114
5900

FIG. 63

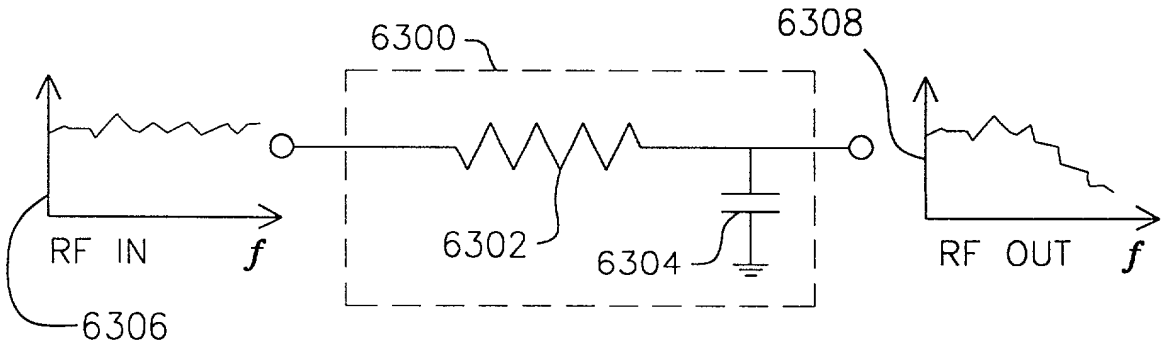


FIG. 64

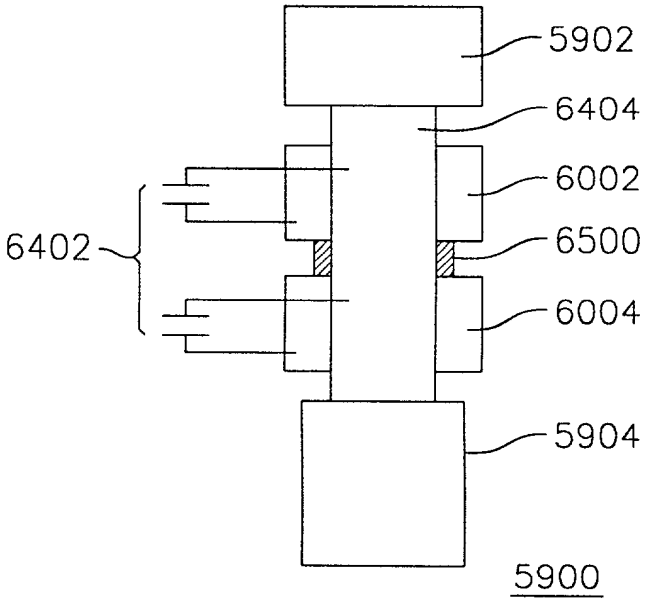


FIG. 65

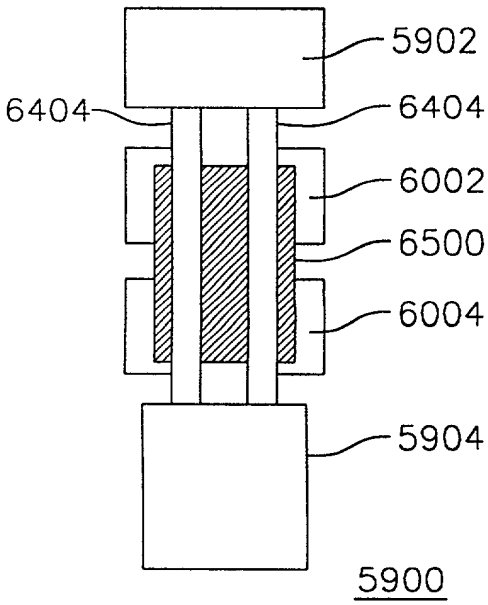


FIG.66

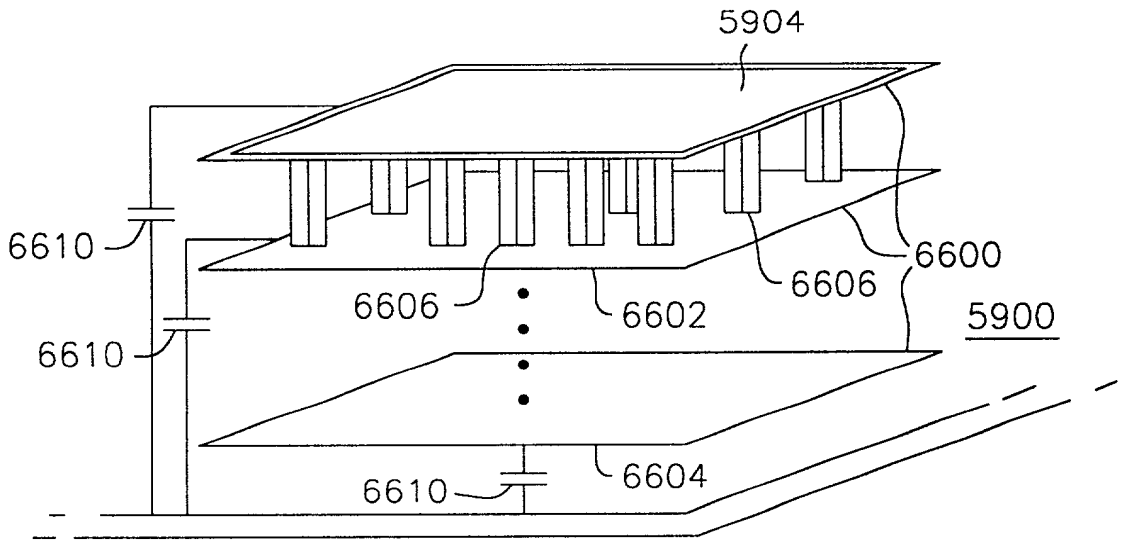

5904
6610
6610
6606
6602
6606
6600
5900
6610
6604

FIG.67

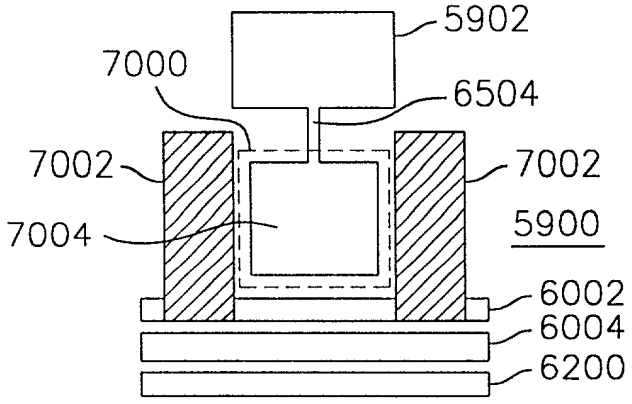

5902
7000
6504
7002
7002
7004
5900
6002
6004
6200

FIG.68

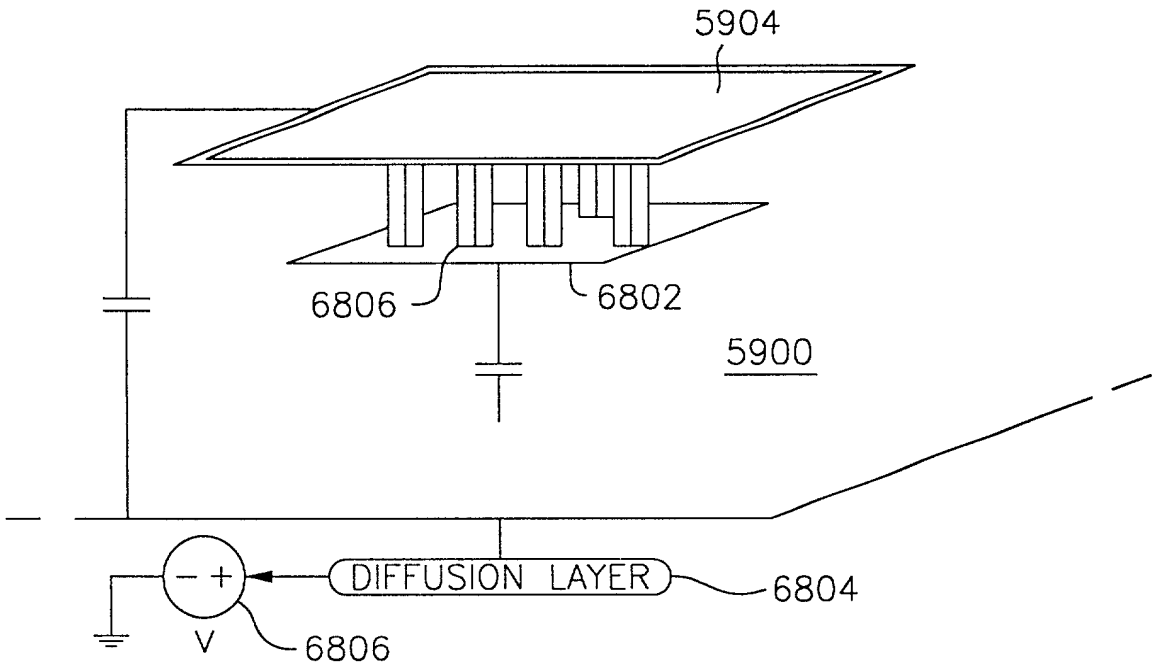


FIG.69a
PRIOR ART

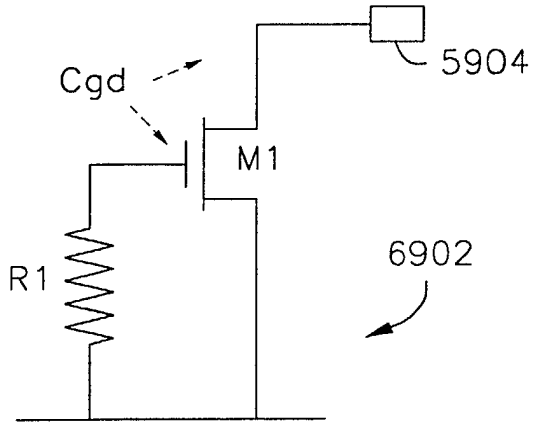


FIG.69b
PRIOR ART

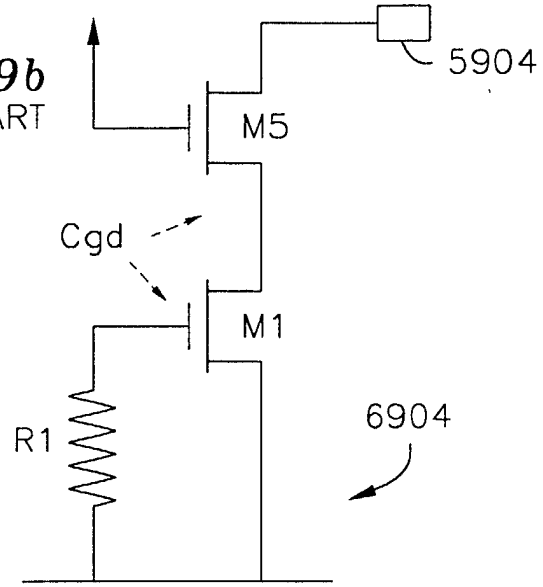


FIG.69c
PRIOR ART

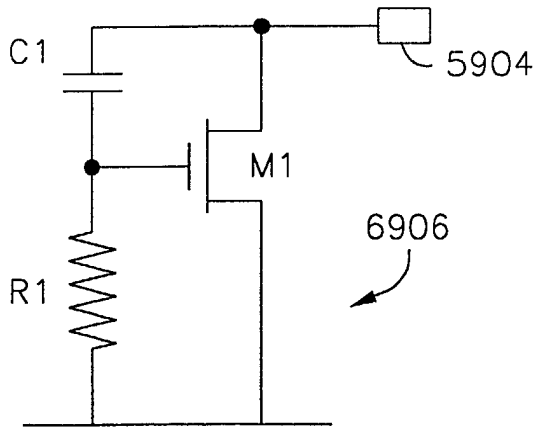


FIG.69d
PRIOR ART

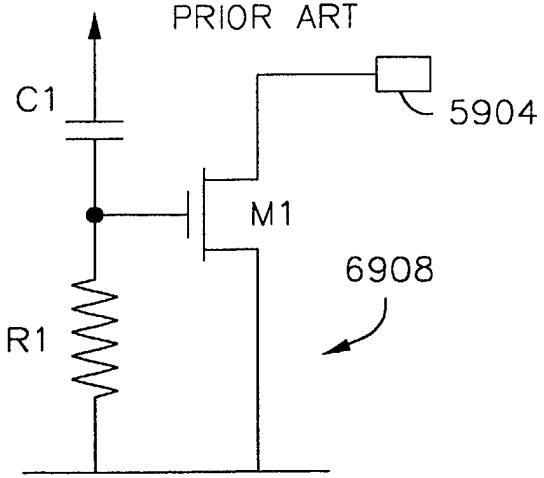


FIG.69e
PRIOR ART

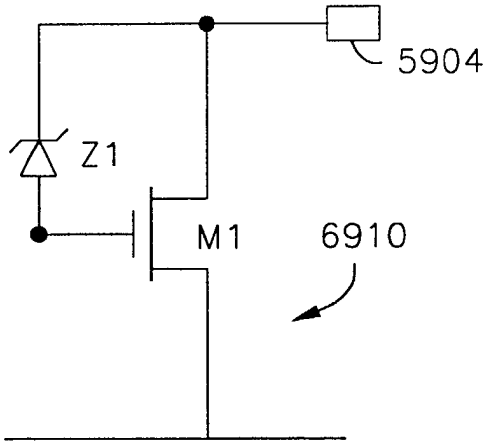


FIG. 70

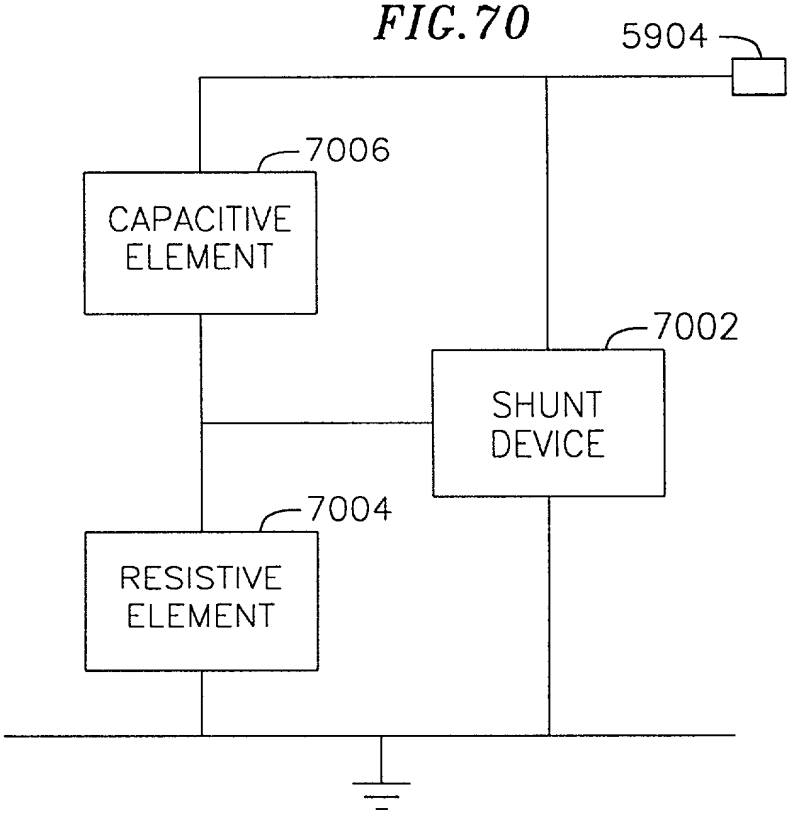

5904
7006
CAPACITIVE ELEMENT
7002
SHUNT DEVICE
7004
RESISTIVE ELEMENT

FIG. 71

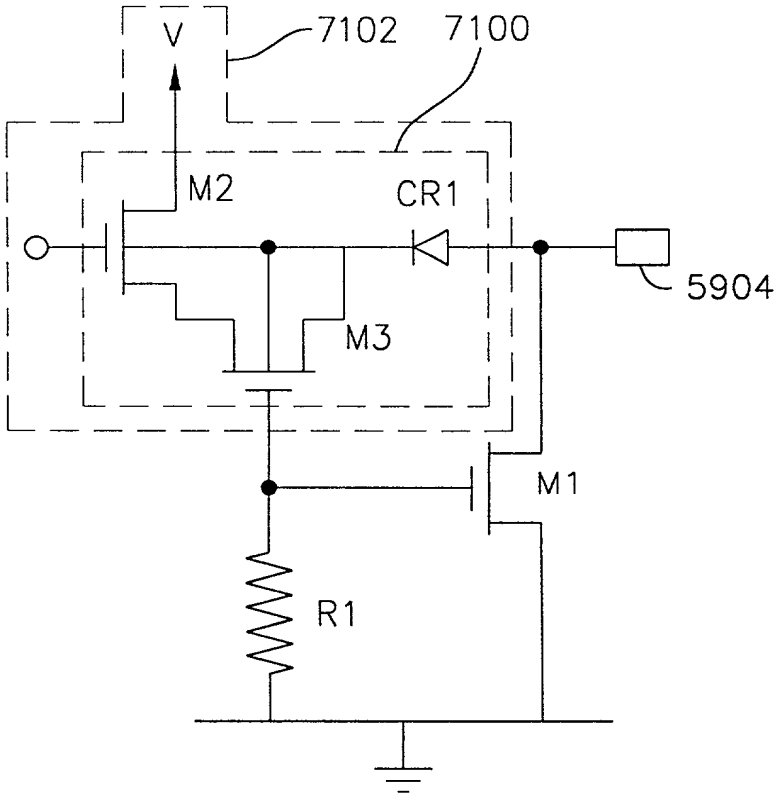

V
7102
7100
M2
CR1
5904
M3
M1
R1

FIG. 72

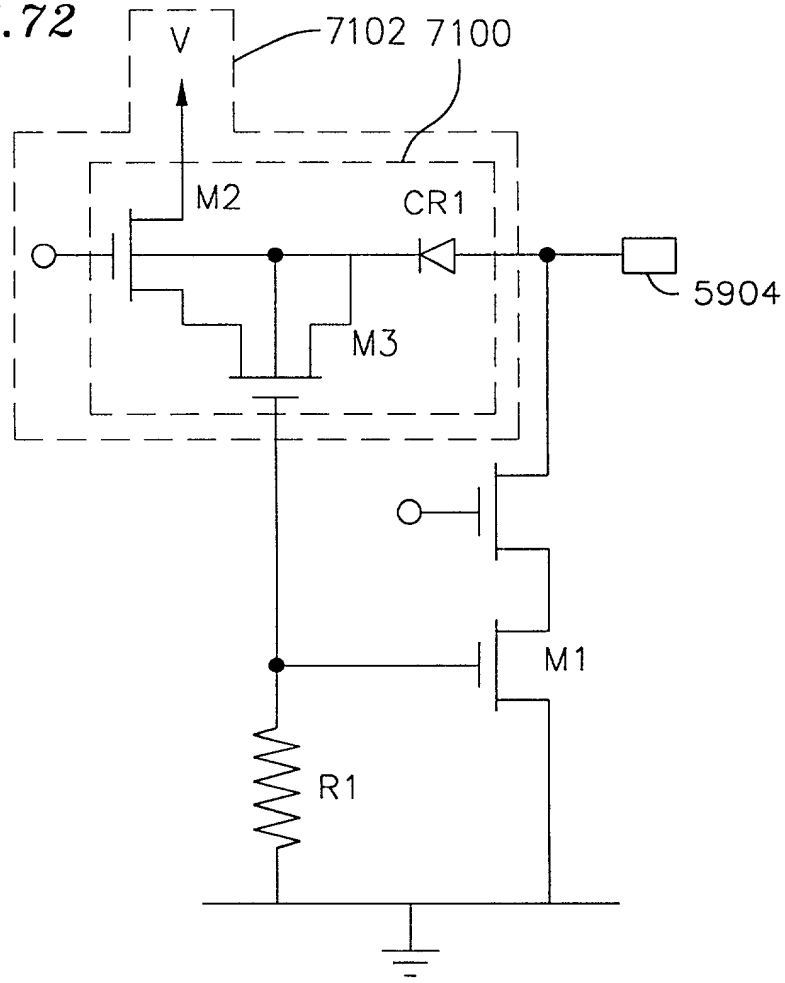


FIG. 73

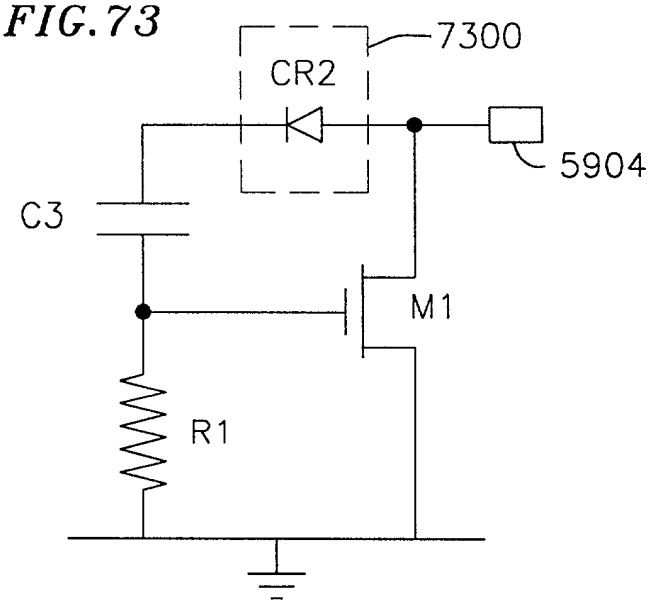


FIG. 74

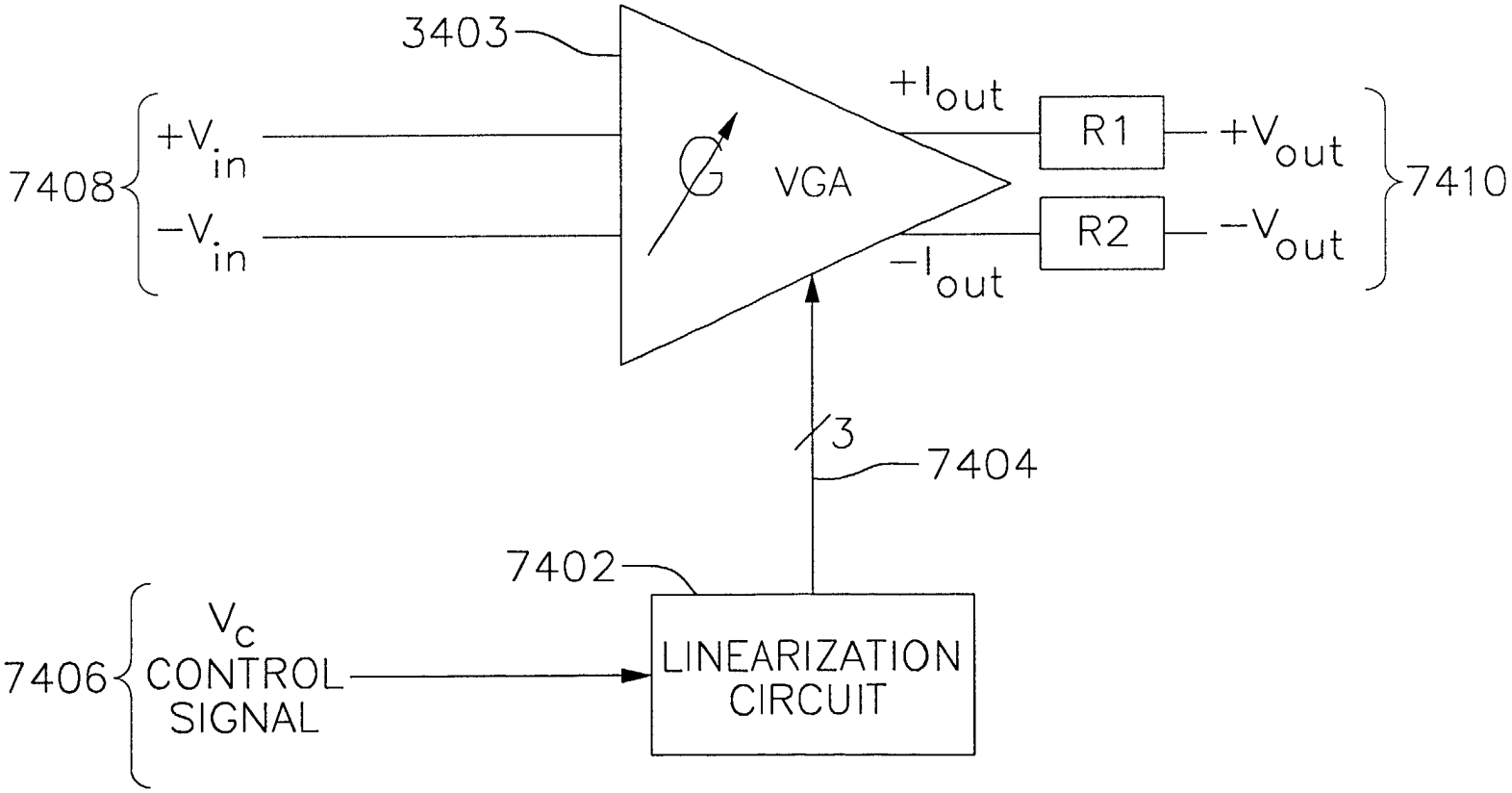
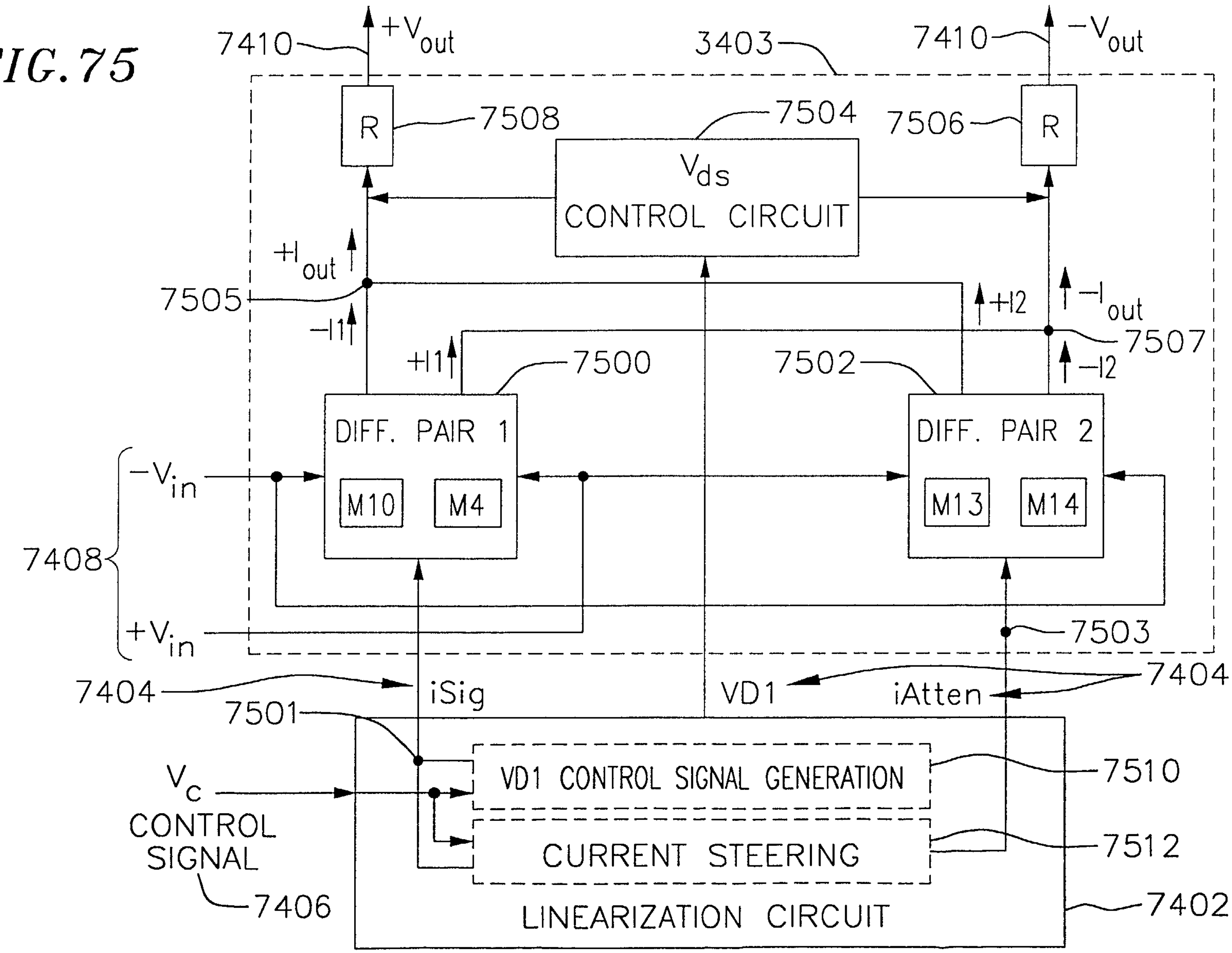

3403
+Iout
7408
+Vin
−Vin
VGA
R1
R2
+Vout
−Vout
7410
−Iout
3
7404
7402
7406
Vc
CONTROL
SIGNAL
LINEARIZATION
CIRCUIT

FIG.75



7410
+Vout
3403
7410
−Vout
R
7508
7504
Vds
CONTROL CIRCUIT
7506
R
+Iout
7505
−I1
+I1
7500
7502
+I2
−Iout
7507
−I2
DIFF. PAIR 1
M10
M4
DIFF. PAIR 2
M13
M14
−Vin
7408
+Vin
7503
7404
iSig
VD1
iAtten
7404
7501
Vc
CONTROL
SIGNAL
7406
VD1 CONTROL SIGNAL GENERATION
7510
CURRENT STEERING
7512
LINEARIZATION CIRCUIT
7402

FIG. 76

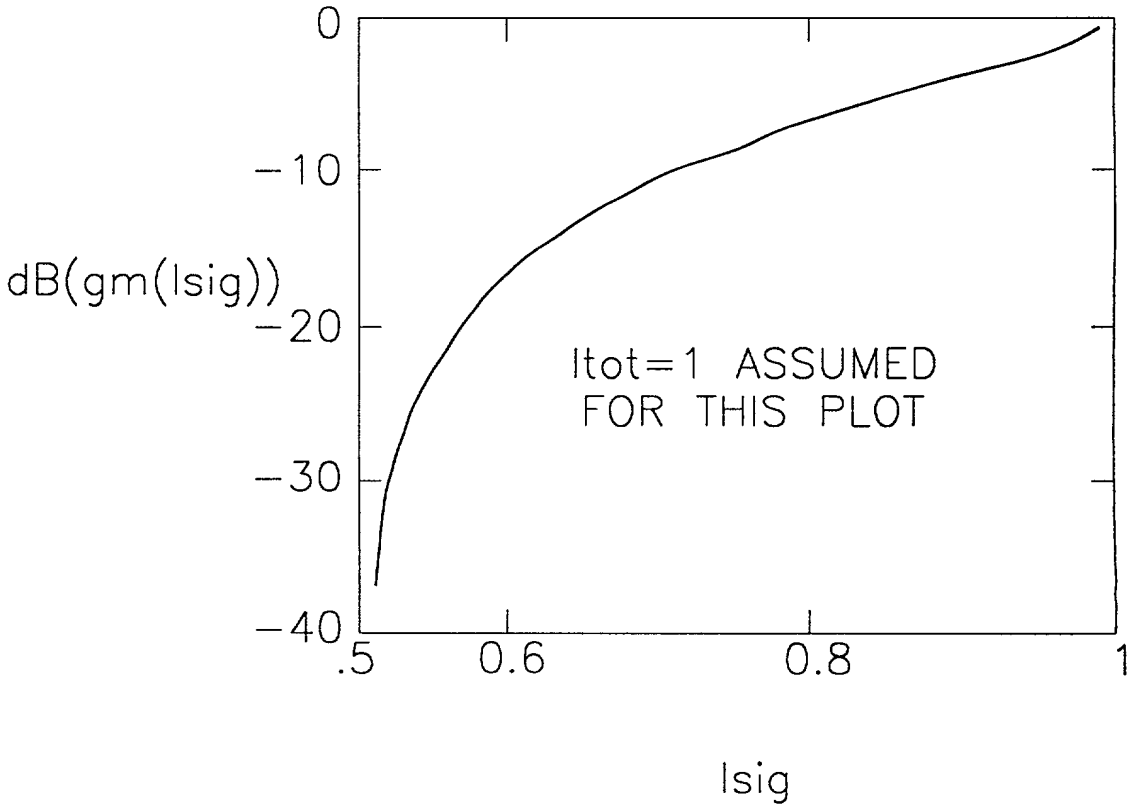

0
−10
−20
−30
−40
dB(gm(Isig))
.5
0.6
0.8
1
Itot=1 ASSUMED
FOR THIS PLOT
Isig

FIG. 77

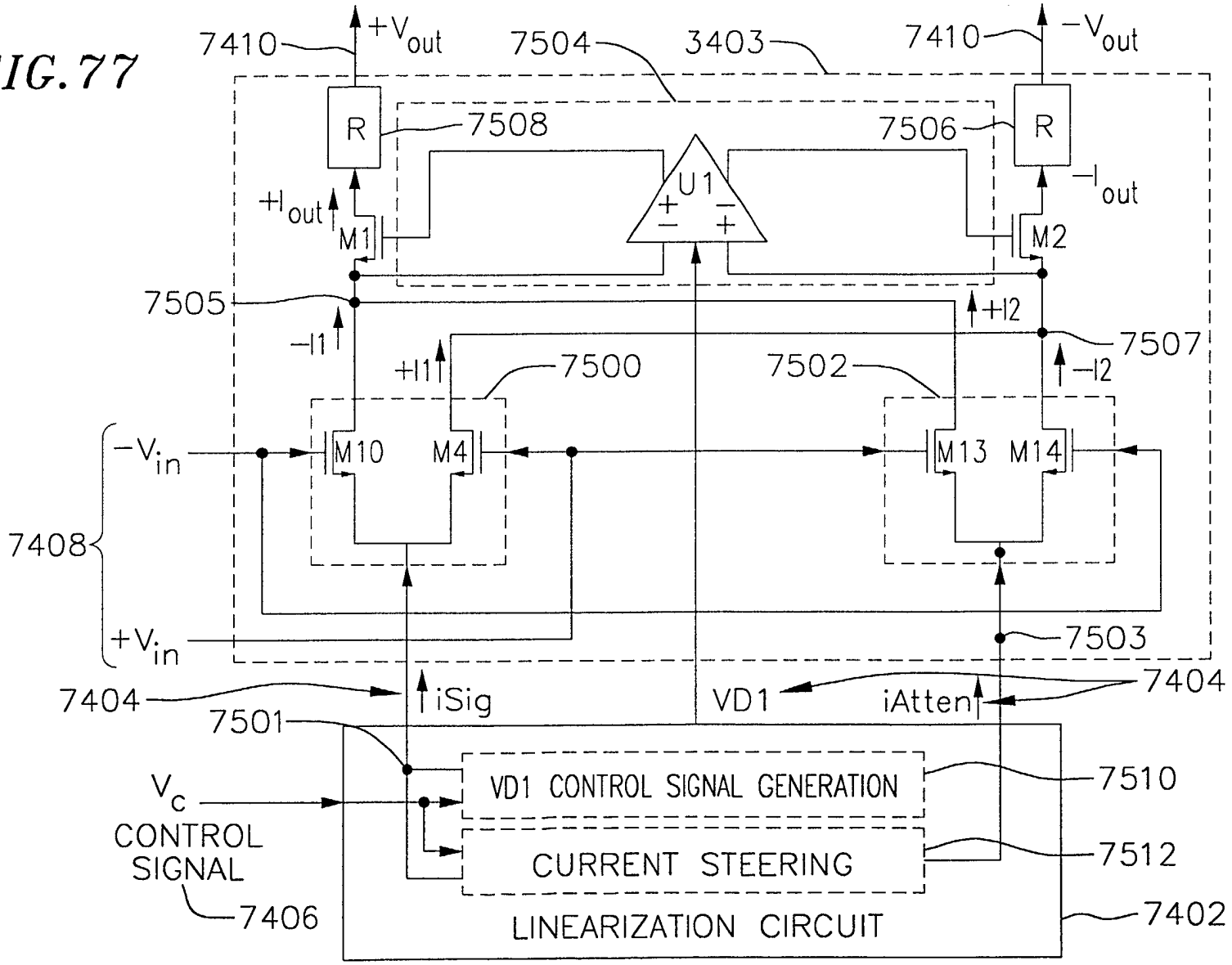

7410
+Vout
7504
3403
7410
−Vout
R
7508
7506
R
U1
+Iout
M1
M2
−Iout
7505
+I2
−I1
7507
+I1
7500
7502
−I2
−Vin
M10
M4
M13
M14
7408
+Vin
7503
7404
iSig
VD1
iAtten
7404
7501
VD1 CONTROL SIGNAL GENERATION
7510
Vc
CONTROL SIGNAL
7406
CURRENT STEERING
7512
LINEARIZATION CIRCUIT
7402

FIG.78a

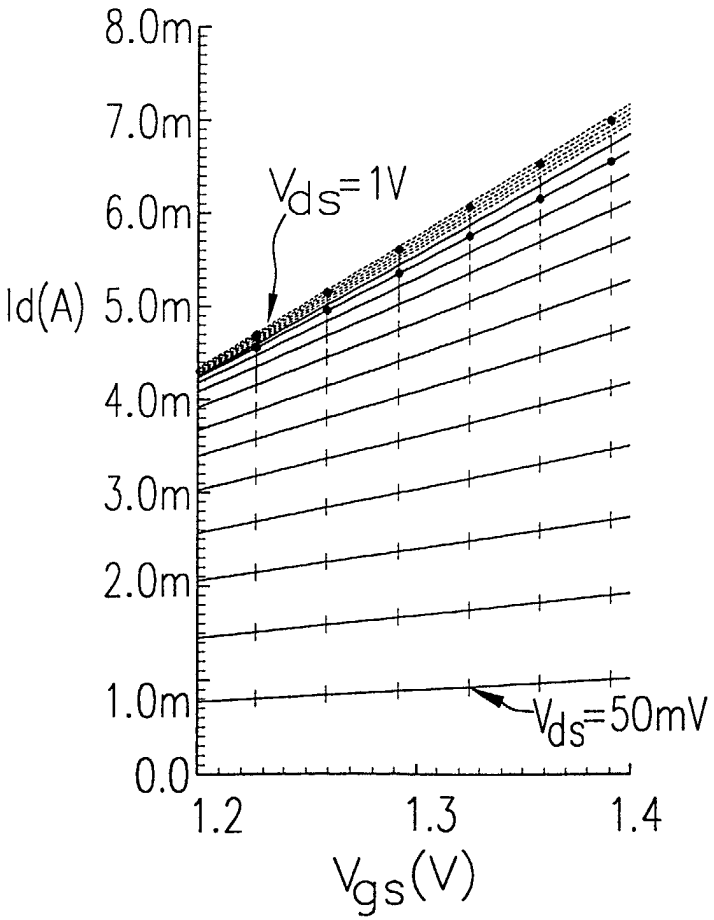


FIG.78b

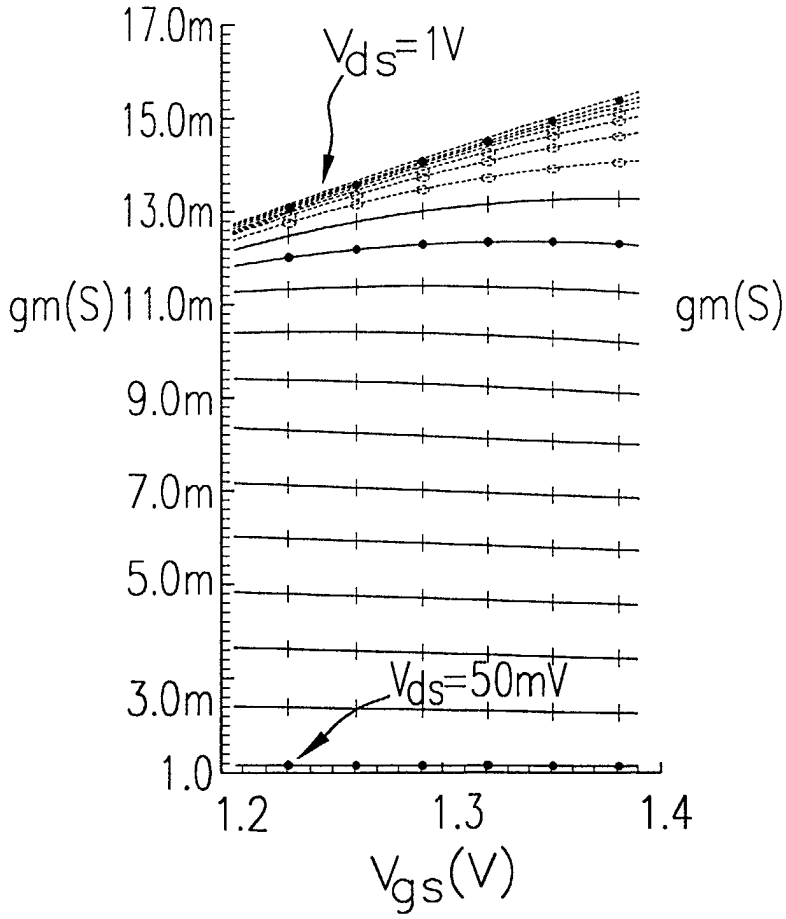


FIG. 78c

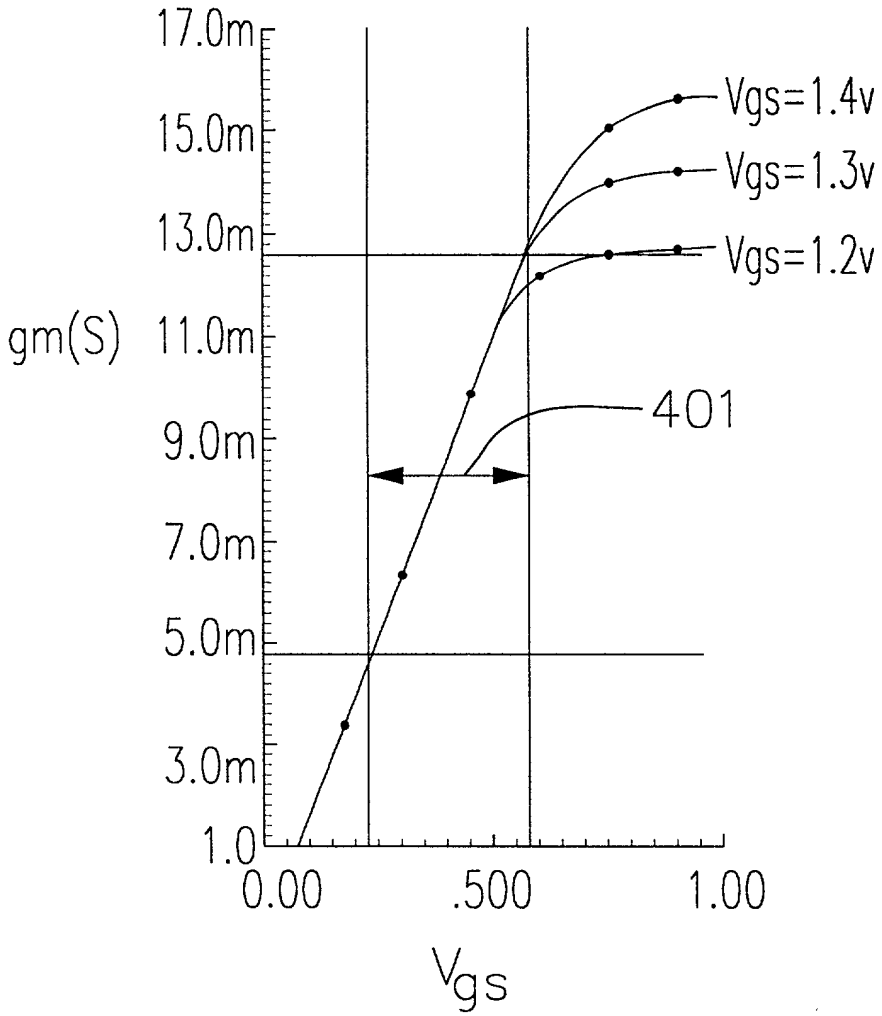

17.0m
15.0m
13.0m
11.0m
9.0m
7.0m
5.0m
3.0m
1.0
gm(S)
0.00
.500
1.00
Vgs
Vgs=1.4v
Vgs=1.3v
Vgs=1.2v
401

FIG.79

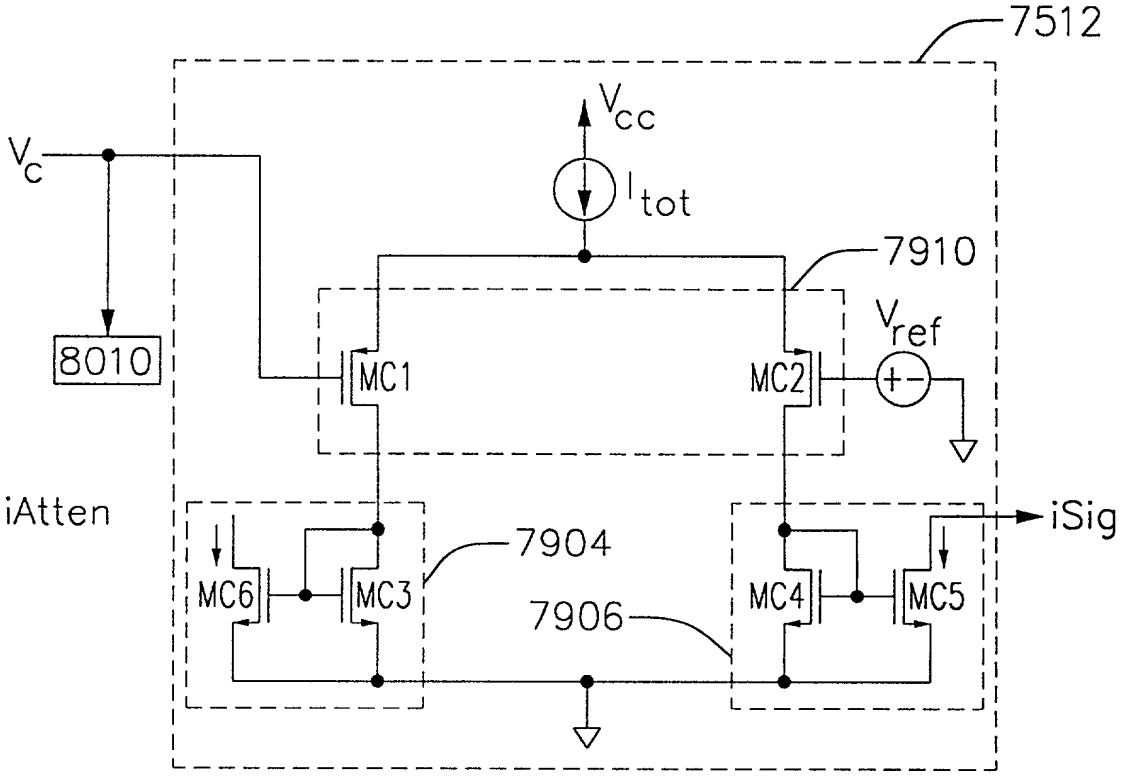
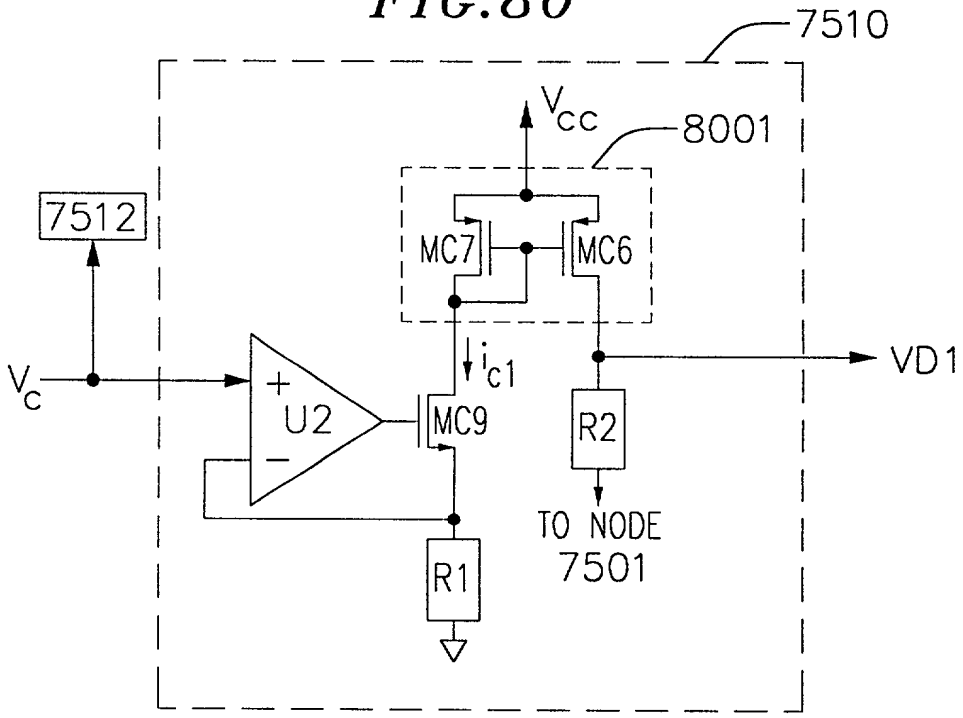

7512
Vcc
Vc
Itot
7910
Vref
8010
MC1
MC2
iAtten
iSig
7904
MC6
MC3
MC4
MC5
7906

FIG.80


7510
Vcc
8001
7512
MC7
MC6
Vc
ic1
VD1
U2
MC9
R2
TO NODE
7501
R1

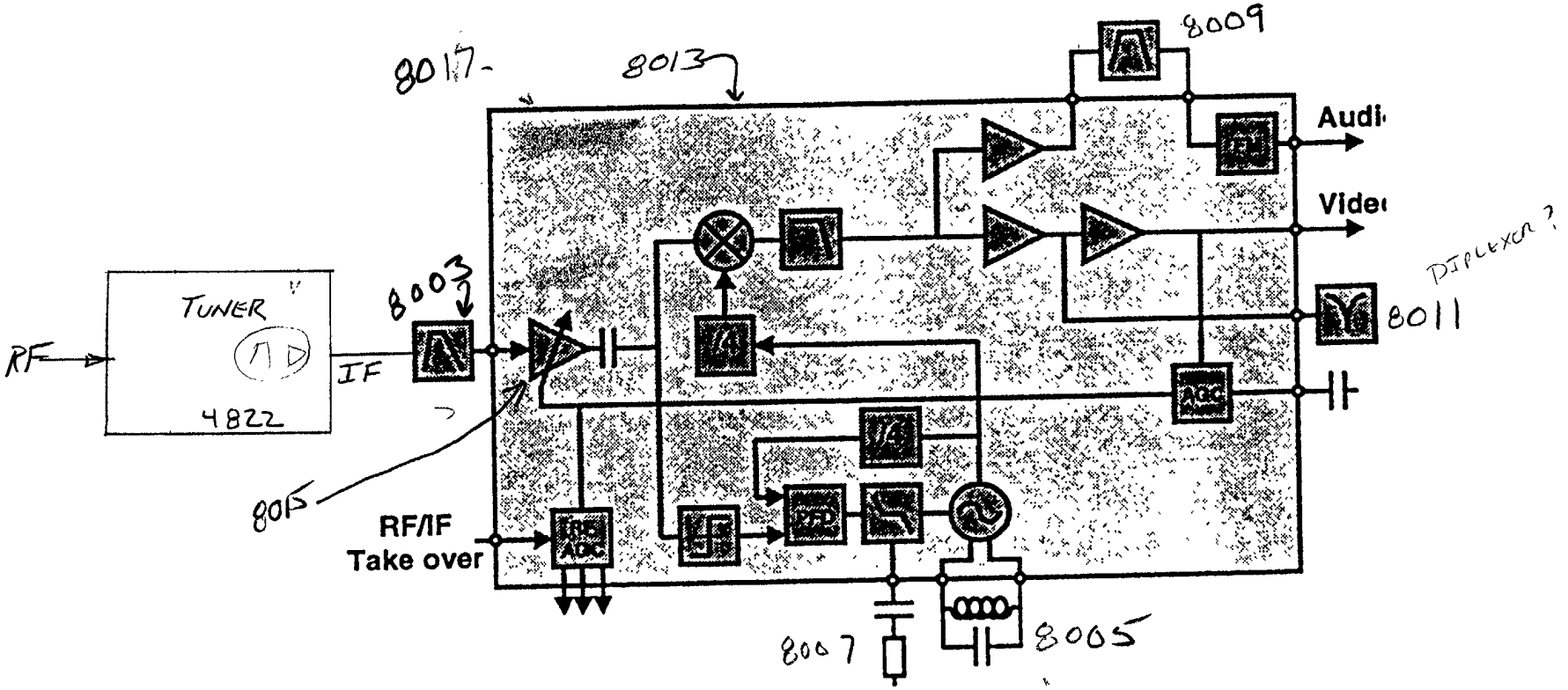

8017
8013
8009
Audi
Vide
DIPLEXER ?
8011
TUNER
RF
IF
4822
8003
8015
RF/IF
Take over
AGC
8007
8005

FIG. 81

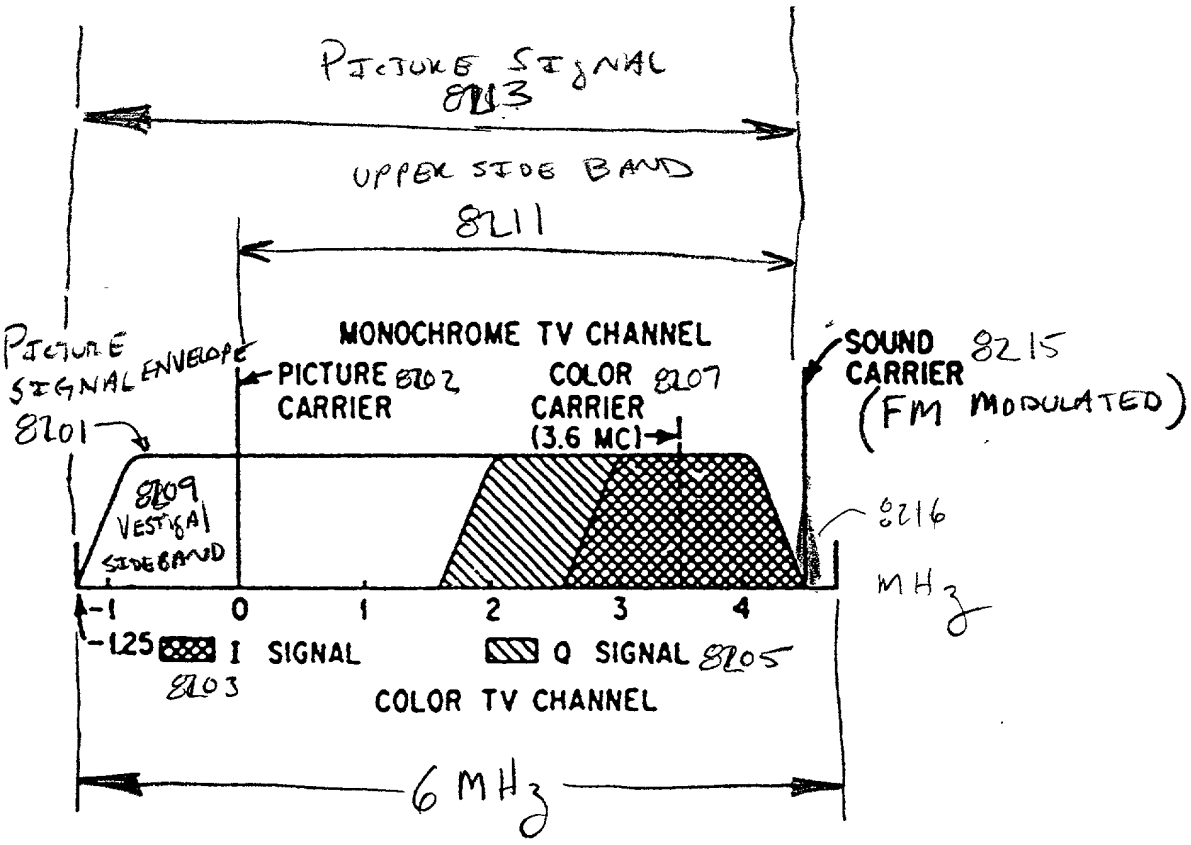

PICTURE SIGNAL
8213
UPPER SIDE BAND
8211
PICTURE SIGNAL ENVELOPE
8201
MONOCHROME TV CHANNEL
PICTURE CARRIER 8202
COLOR CARRIER (3.6 MC) 8207
SOUND CARRIER 8215
(FM MODULATED)
8209
VESTIGIAL SIDEBAND
8216
MHz
-1
0
1
2
3
4
-1.25
I SIGNAL
8203
Q SIGNAL 8205
COLOR TV CHANNEL
6 MHz

FIG. 82

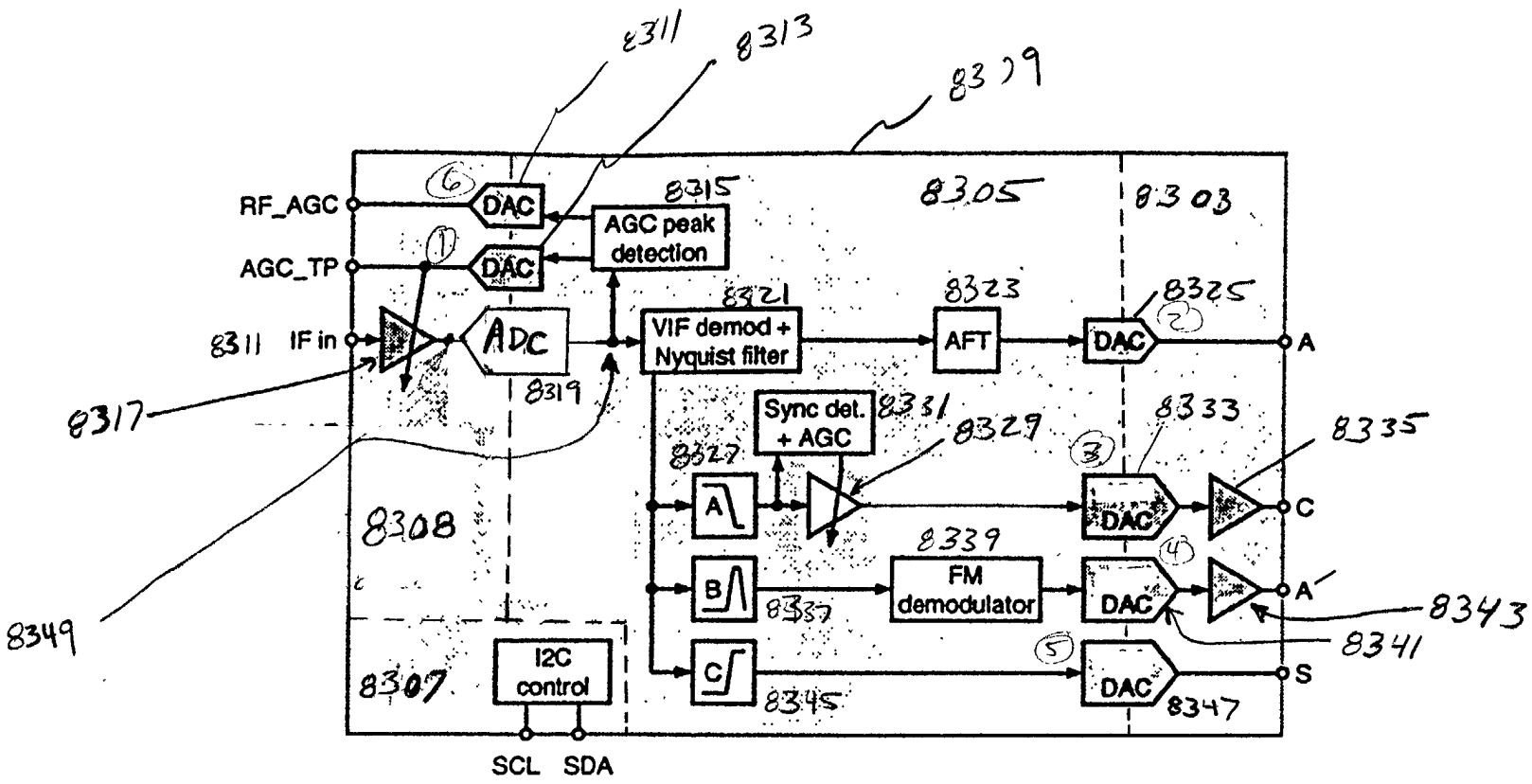


FIG. 83

FIG. 84a

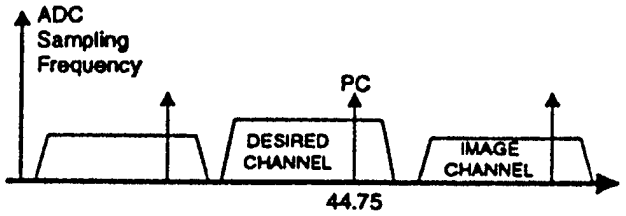


FIG 84b

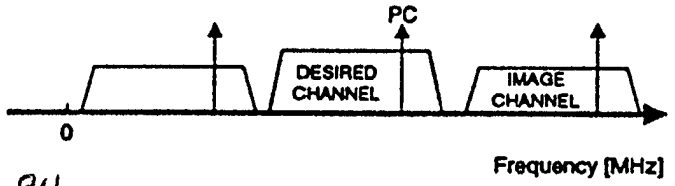


FIG 84c

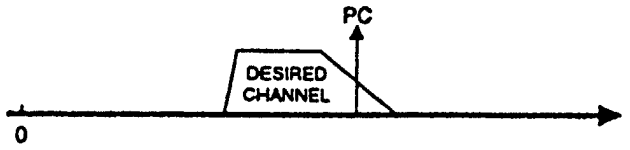
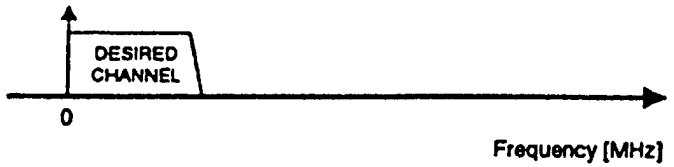


FIG 84D



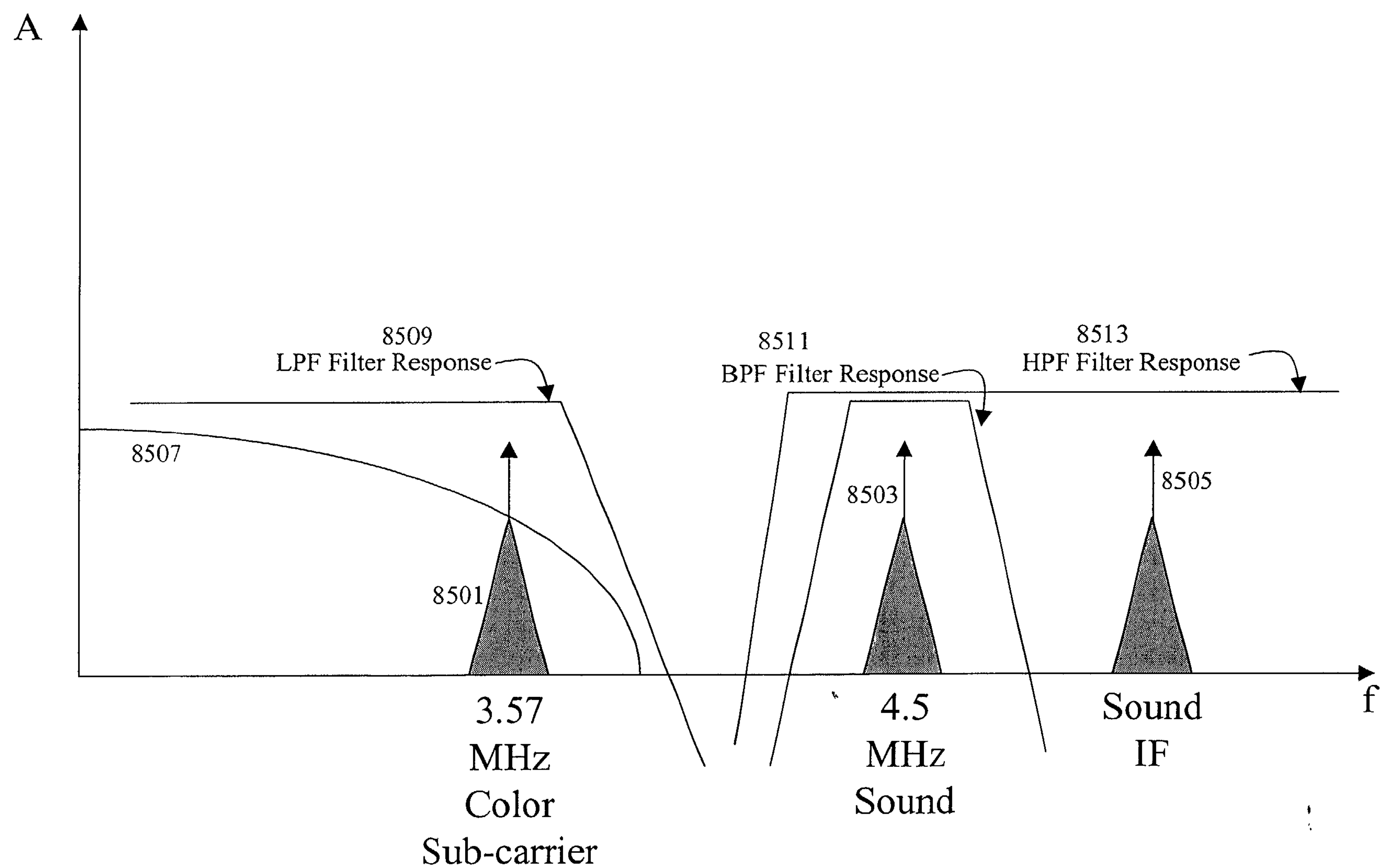

A
8509
LPF Filter Response
8511
BPF Filter Response
8513
HPF Filter Response
8507
8501
8503
8505
3.57
MHz
Color
Sub-carrier
4.5
MHz
Sound
Sound
IF
f

FIG. 85